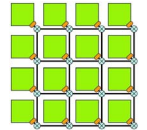
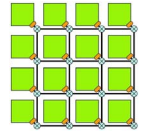
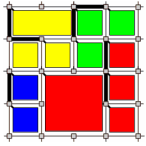


Two words from our sponsors...

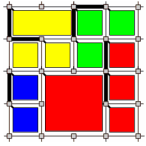


- Send us PDF of your poster
 - We want to post it on the web with the abstract and the other presentations
- Fill out the feedback questionnaires
 - This is not just for DATE: We will read your feedback first !

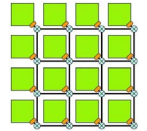


NoC 2007 and Beyond:

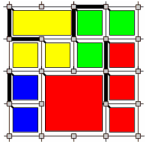
Proposal for an IEEE Symposium



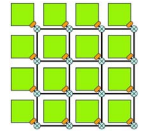
This is a Proposal



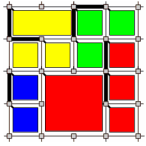
- All items are only proposals, subject to discussion
 - This presentation will be posted on the NOC2006 web site
- Suggestions welcome!
 - Please email feedback to Ran Ginosar
 - Email address on same web site



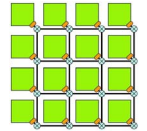
Agenda



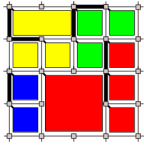
- Type of symposium
- Type of papers
- Technical Program Committee
- Steering Committee
- IEEE sponsorship
- Proposals for 2007 and beyond
- Scope for the symposium



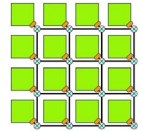
Type of Meeting



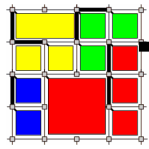
- Symposium
 - Not an informal workshop (unlike NOC2006)
 - “Almost” a conference
 - To be named: IEEE International Symposium on Networks on Chip (NoC)
 - Must be applied to and approved by the IEEE
- High quality
- Target acceptance rate less than 1/3
- One track—no parallel sessions
- 25 minute presentations, 5 minutes questions
- Length 2 ½ days (range 2–3½ days)
 - E.g. 8 sessions, 3 papers each, total 24 papers



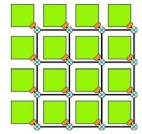
Papers



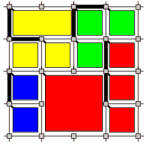
- 6-10 pages
 - Extra payment for 1 or 2 extra pages
- Original research results
- Usual IEEE publication and archiving process
 - Papers posted on IEEE *Xplore*
- Typical time-table:
 - Submit 6 months before conf
 - Review in 3 weeks, discussions and decisions in 3 weeks
 - Camera ready 2 months before conf (IEEE Press rules)



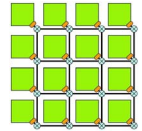
Technical Program Committee



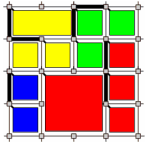
- Each paper reviewed by 4-5 TPC members
 - Sub-reviewers allowed, but responsibility on TPC members
- Submission and review: Blind or not ?
- TPC Meeting
 - Either discussions by email
 - Or a physical meeting (e.g. during DATE)



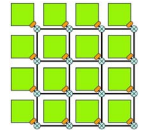
Steering Committee



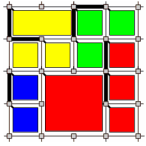
- Will follow standard IEEE charter
- Rotating:
 - General and TPC chairs will join each year
 - There will be a phase out rule
 - Typical term around 5 years
- Steering Committee tasks
 - Solicit proposals for
 - Location
 - General chair(s)
 - TPC chair(s)
 - Select and nominate location / GC / TPC chairs
 - Determine policies



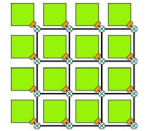
Initial Steering Committee Proposal



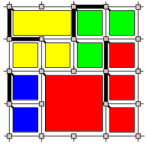
- Ran Ginosar, Technion (org. NoC2006)
- Pol Marchal, IMEC (org. NoC2006)
- Alex Yakovlev, NCL (org. NoC2006)
- Axel Jantsch, KTH
- Giovanni de Michelli, EPFL
- Kees Goossens, Philips
- Wayne Wolf, Princeton (prop. 2007 GC)
- Eby Friedman, Rochester (prop. 2007 GC)
- Avi Kolodny, Technion (prop. 2007 TPC)
- Li-Shiuan Peh, Princeton (prop. 2007 TPC)



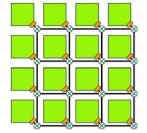
IEEE Sponsorship



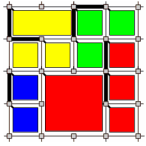
- Proposed: Through CEDA
 - The new Council on EDA
- Benefits
 - Publication on IEEE *Xplore*
 - Reputation
 - Rules for orderly conduct
 - Advance money for conferences
 - Conference insurance
 - Financial audit and control
- Drawback (minor)
 - IEEE takes 14% of intake



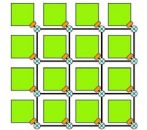
2007 Proposal



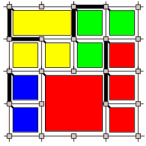
- Location: Princeton, NJ
- Time: May 2007
- General Chairs:
 - Wayne Wolf, Princeton University
 - Eby Friedman, University of Rochester
- TPC Chairs:
 - Avi Kolodny, Technion
 - Li-Shiuan Peh, Princeton



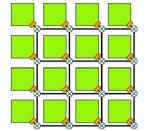
Future Years



- Geographical rotation
- 2008: Europe ?
- 2009: Far East or USA?
- 2010: Israel ?



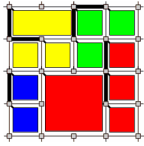
Topics of Interest



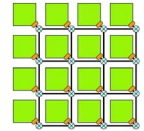
System

NoC

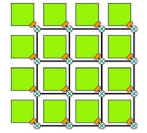
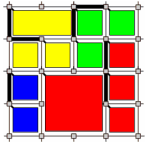
interconnect



Example Topics



- Network issues in NoC
- Power issues
- NoC architecture
- NoC for MPSoC and App. Specific SoC
- Case studies
- Clocking and synchronization for NoC
- Arbitration
- Interconnect (metal, optical, 3D)
- Synchronous and Asynchronous NoC
- Reliability
- Quality of Service
- Memory and caches on NoC
- Circuits for NoC
- Wires and Interconnect
- Testing of NoC
- Testing of modules using the NoC
- Reliability
- Symmetric and Asymmetric MP NoC
- Technology issues
- NoC for FPGA and Structured ASIC
- NoC design methodology, design flow and tools
- EDA for NoC design
- NoC simulation and performance evaluation
- Modeling and analytical studies of NoC
- Formal verification of NoC design
- Formal design methods
- Applications that benefit from / require NoC
- router & NI architectures,
- End-to-end issues: Congestion, Flow Control,
- Run-time issues
- Programming models
- NoC over multiple chips



Thank you
Have a safe flight home!

