A Design-for-Test Implementation of an Asynchronous Network-on-Chip Architecture and its Associated Test Pattern Generation and Application

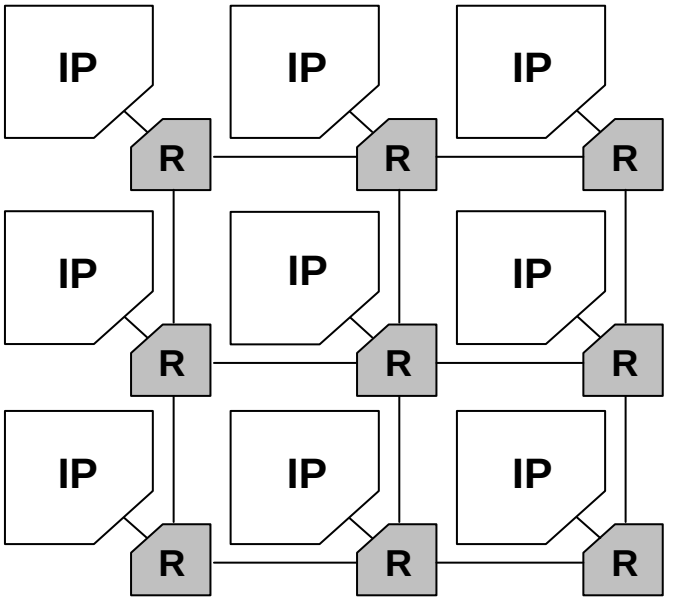
VNU-COLTECH
Xuan-Tu Tran
tutx@vnu.edu.vn

CEA-LETI
Yvain Thonnart
Jean Durupt

INPG-LCIS
Vincent Beroulle
Chantal Robach

Network-on-Chip Testing

- **Test of network architecture (routers and links)**
  - ✗ Low controllability and observability
    - Especially for the routers who are far from primary inputs/outputs
  - ✗ Network links & routers are implemented in asynchronous logic
  - ✓ Routers are regular & identical



- **Test of IPs and their network interfaces**
  - Using classical techniques: IEEE 1500, scan chains, etc.
  - Network architecture can be used as a Test Access Mechanism (TAM)
    - *High bandwidth*
    - *No additional cost for the TAM*
    - *Test patterns must be encapsulated in packets*

Presentation outline

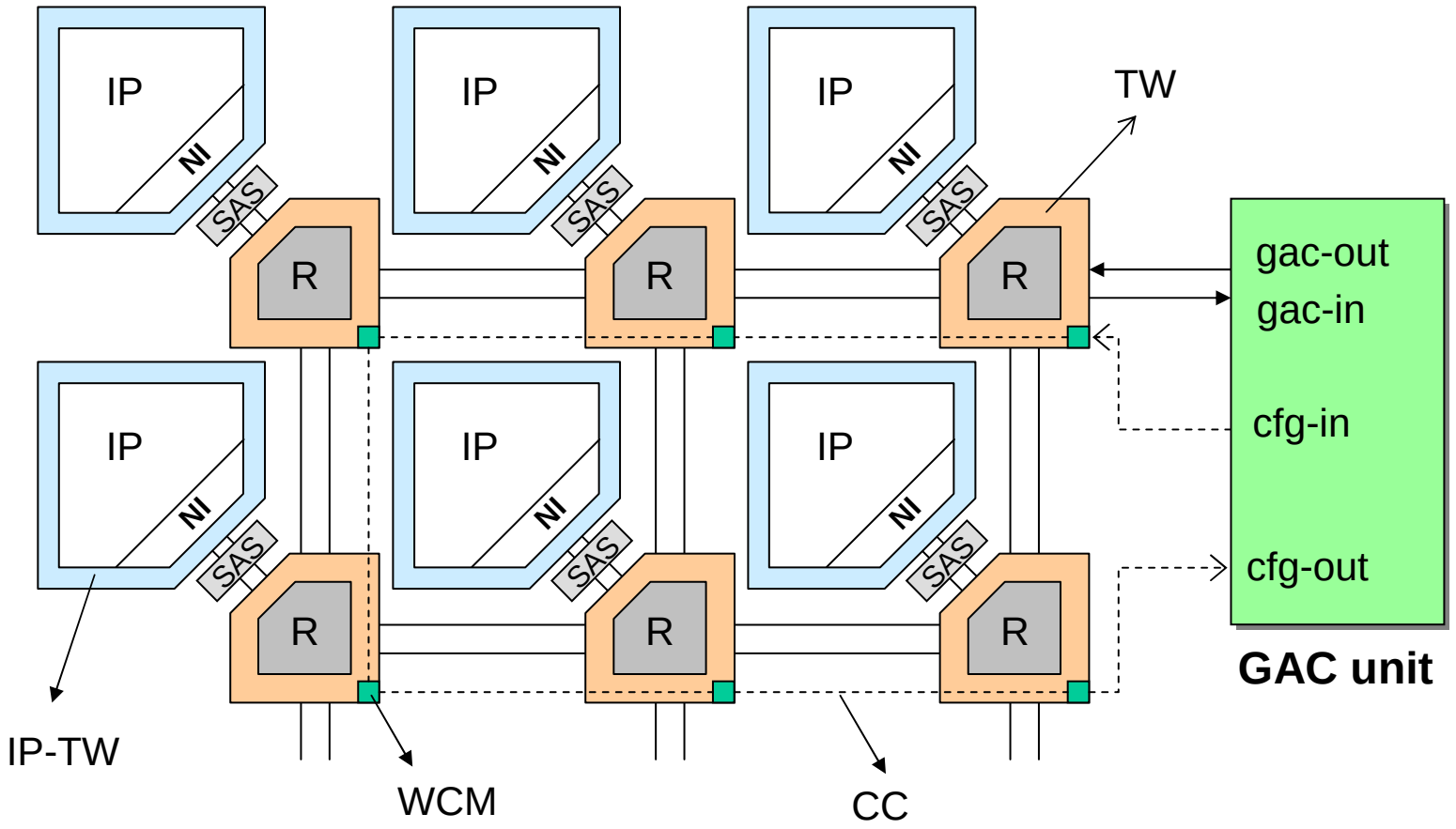
- **Proposition of a DfT architecture for asynchronous NoCs**
- **Application the developed DfT architecture to ANOC network**
- **IP cores testing with the proposed DfT architecture**
- **Conclusions et perspectives**

Test method for asynchronous NoCs

	Structural test	Functional test
Classical utilization for synchronous circuits	■ **Production test** ✓ Well-known techniques ✓ Many available tools	■ **Verification and/or production test** ✗ knowledge of the functionality of circuits-under-test is needed
Application to asynchronous NoCs	✗ **High test overhead** • DfT expensive in area • Lack of CAD tools • Back-end difficult [Efth05T, Ronc94P, Petl95S,Garc98S]	✓ **Simple functionality** • Interconnection structure • Test vectors are easily generated ✗ **Low controllability, low observability**

☺ **Functional test with wrappers**

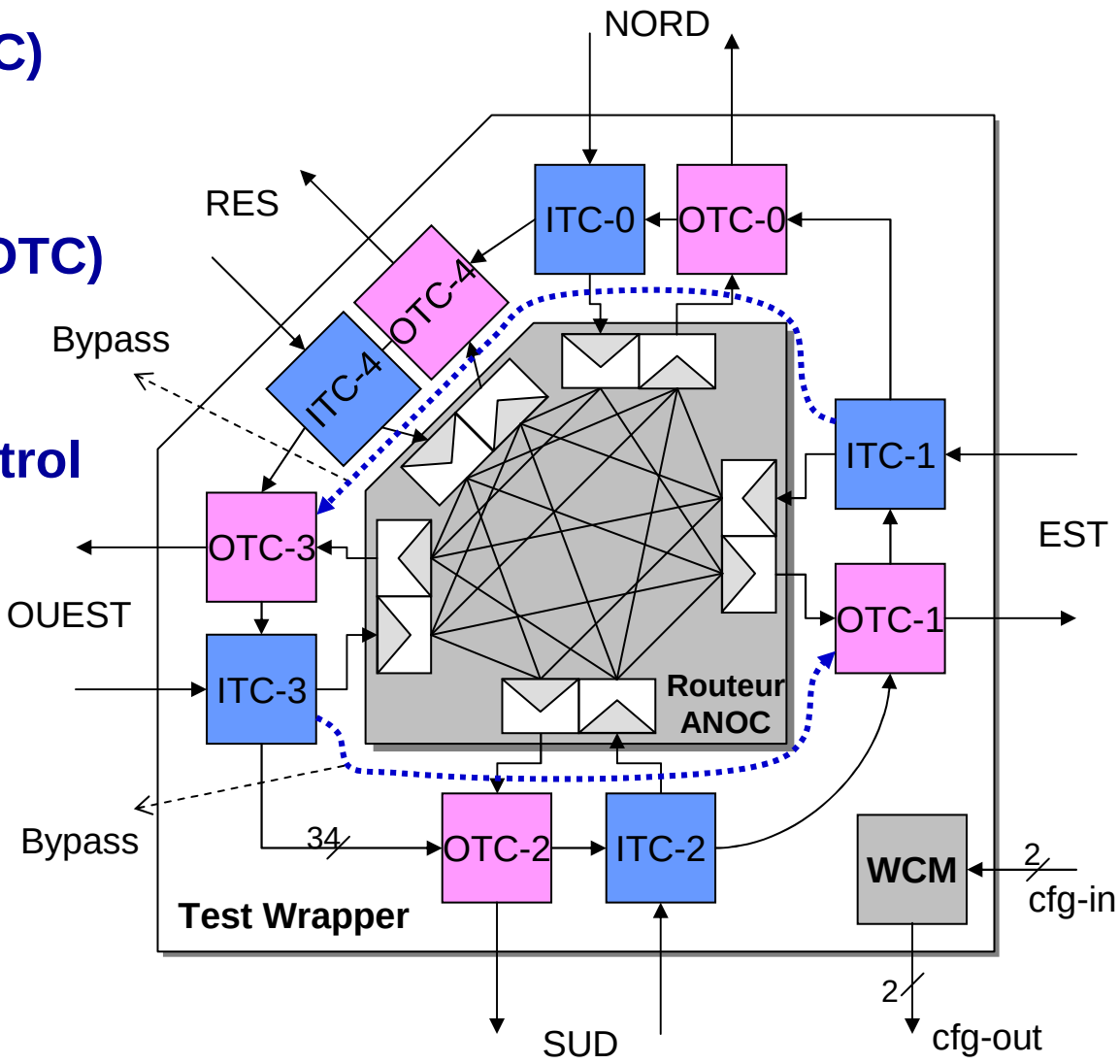
Proposition of an asynchronous DfT architecture



- Test Wrapper (TW)
- Wrapper Control Module (WCM)
- 2-bit configuration chain (CC)
- Generator-Analyzer-Controller (GAC)
- Synchronous/Asynchronous Interface (SAS)
- Network Interface (NI)
- Router (R)
- IP Test Wrapper (IP-TW)

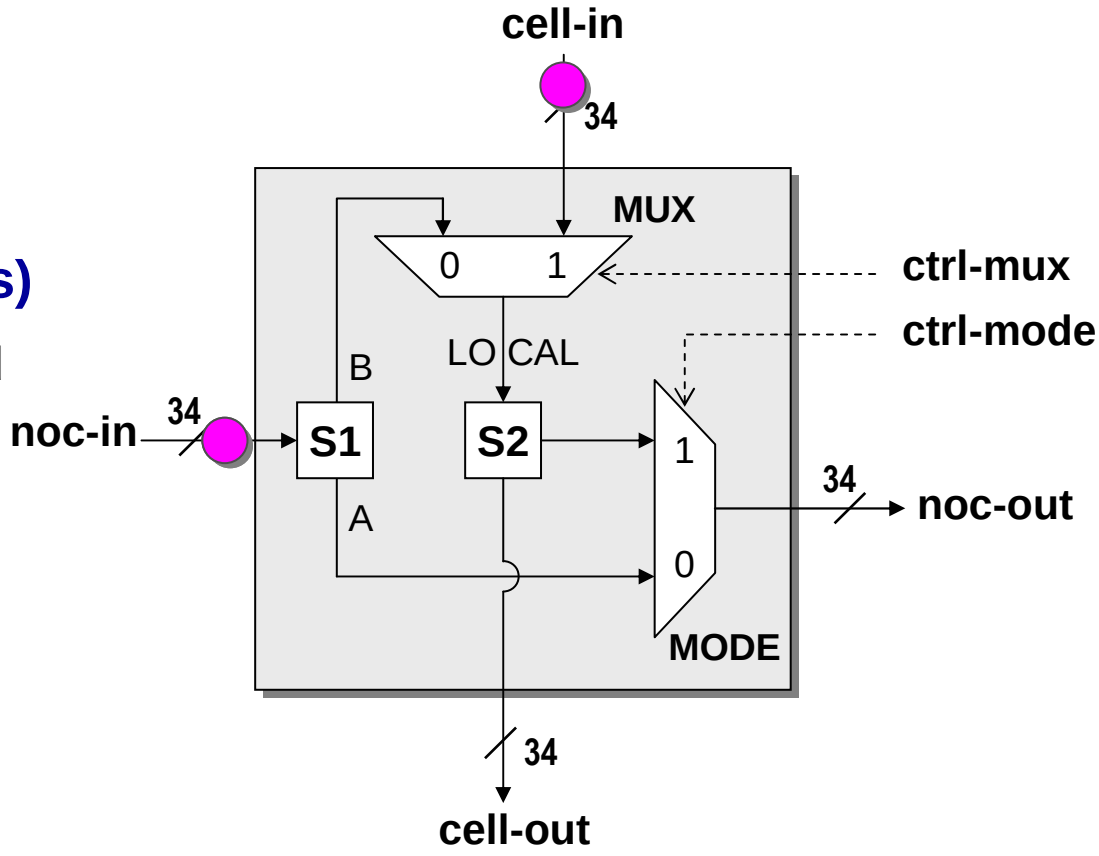
Test Wrapper Architecture

- **5 input test cells (ITC) for the inputs**
- **5 output test cells (OTC) for the outputs**
- **A local wrapper control module (WCM)**
- **Bypass function**



Test cell micro-architecture

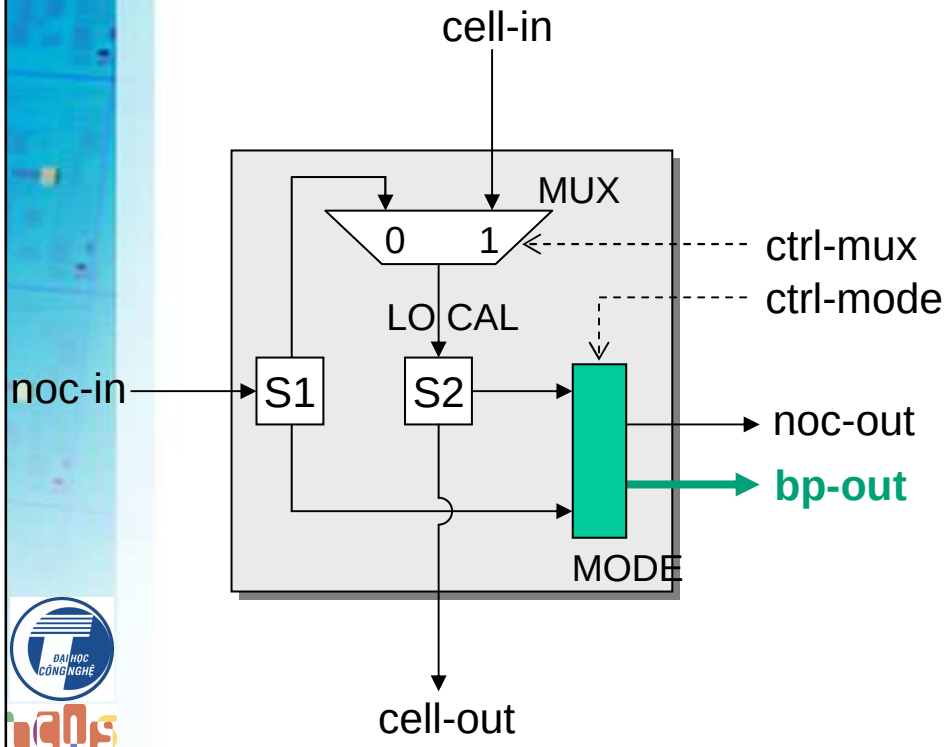
- **2 multiplexers**
- **2 combinational splits (separation blocks without control signals)**
  - Input data is presented at both outputs
  - This data is acknowledged by the receiver who needs it



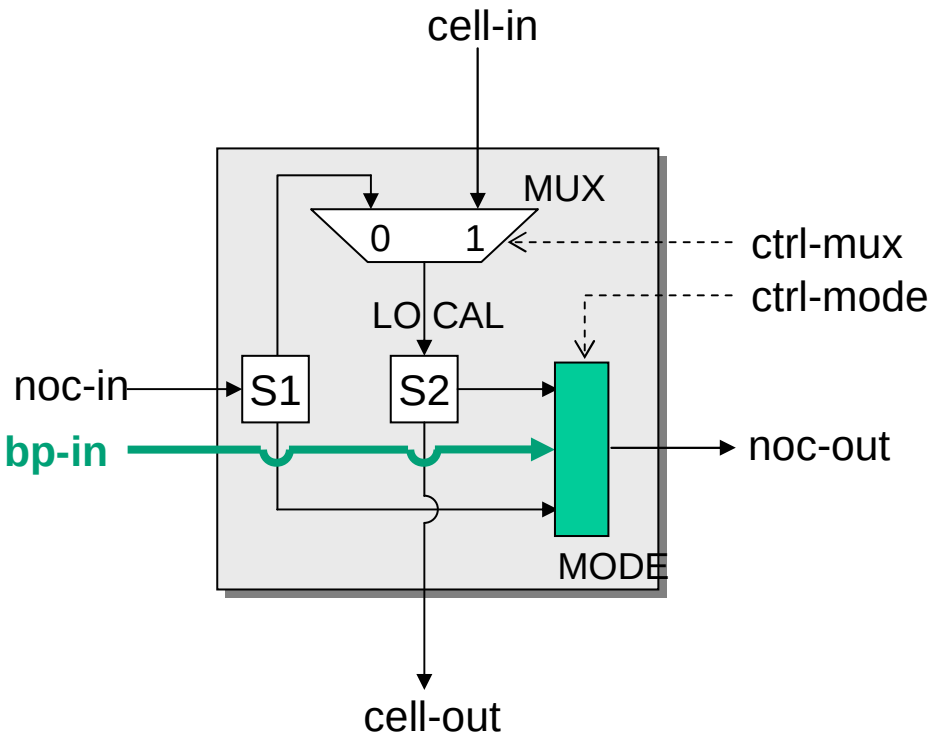
(test cell micro-architecture, for both ITC & OTC)

Test cell micro-architecture with “bypass” function

- **Implementation of a test cell with “bypass” function**
  - Add an output port for input test cells
  - Add an input port for output test cells



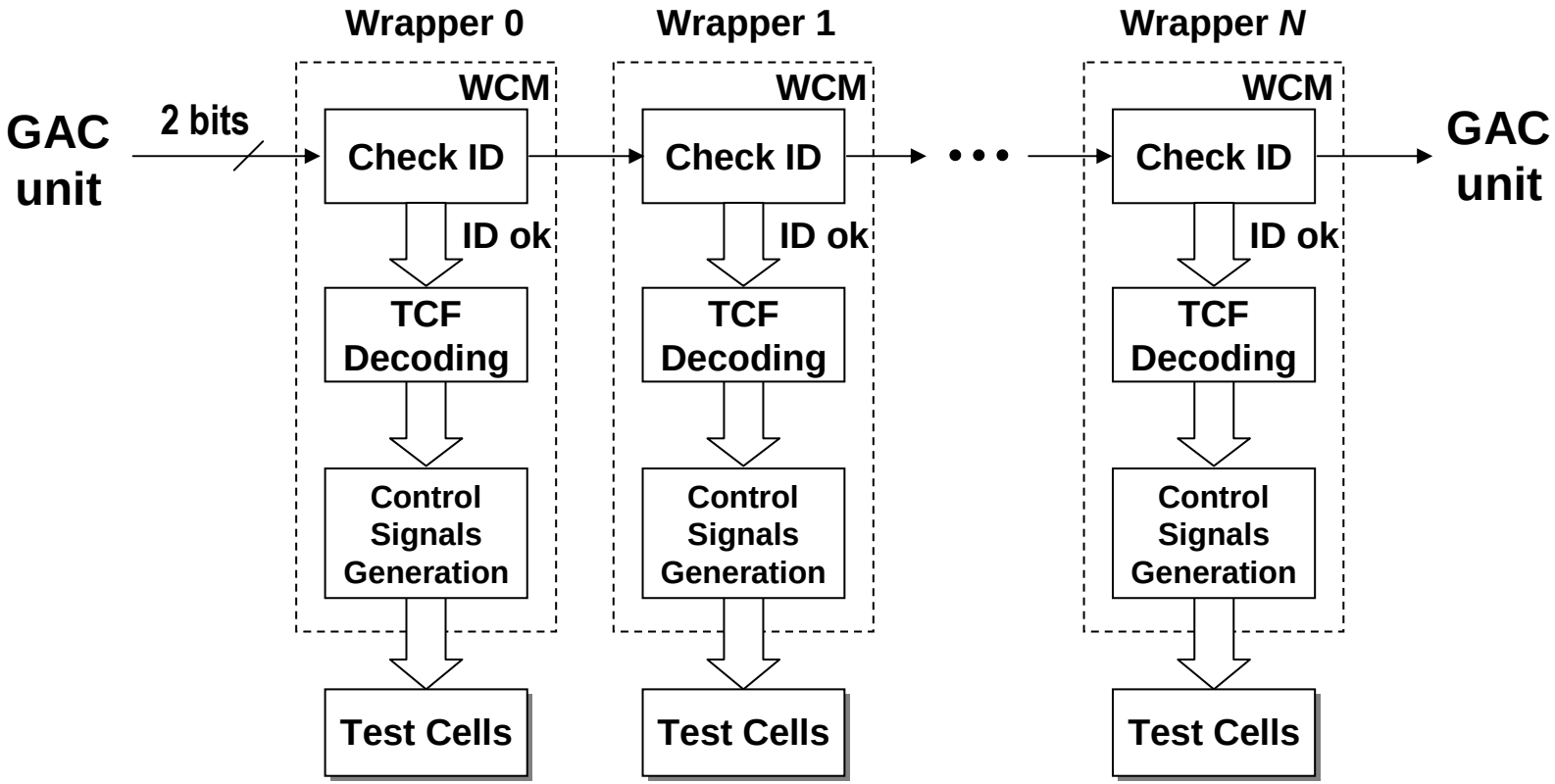
(Input Test Cell - ITC)



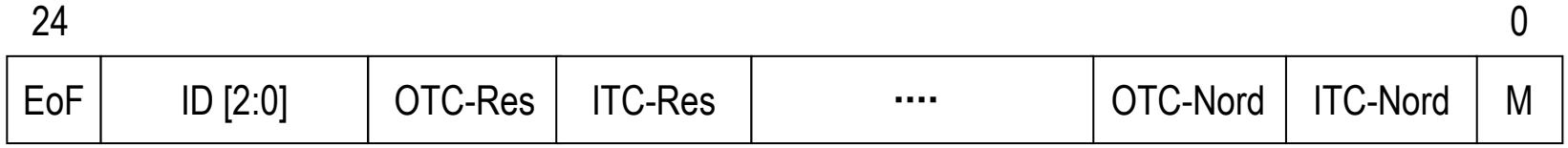
(Output Test Cell - OTC)

Configuration chain architecture

Configuration chain

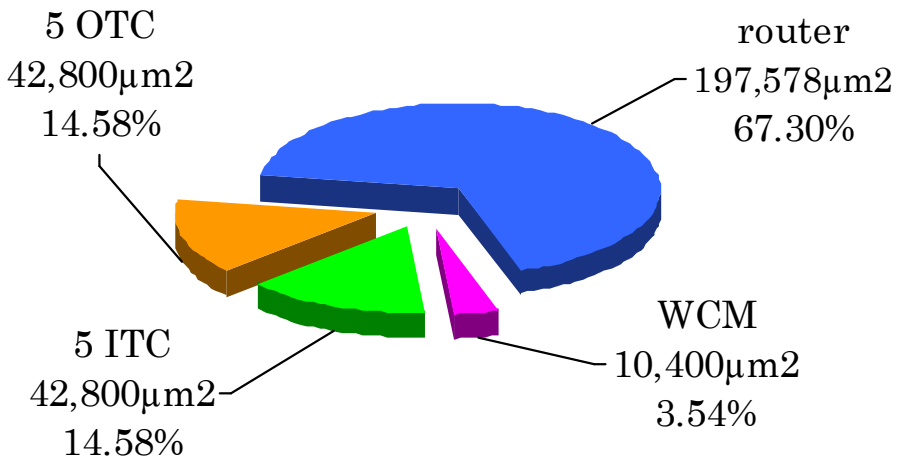


Test configuration frame



Implementation and results (1/2)

- **STMicroelectronics 65*nm* technology**
  - With the standard asynchronous cell library (TAL065) from the TIMA laboratory
- **Area overhead**



  - 32.7% of a testable router
  - 3 → 5% of the total surface of a System-on-Chip

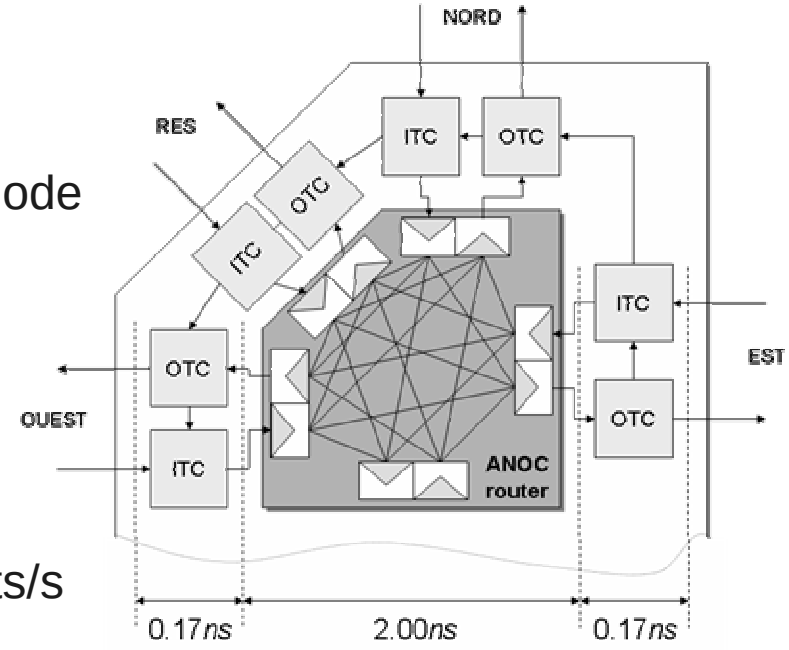
Implementation and results (2/2)

Test bandwidth

- Maximum throughput: 20M-vectors/s
- Normal throughput: 10M-vectors/s

Added latency

- Communication latency in normal mode increased of 0.17ns per test cell



Maintained throughput

- Communication throughput in normal mode maintained at 500Mflits/s

Integrated into a test chip

- functionality & performance validated

Presentation outline

- Proposition of a DfT architecture for asynchronous NoCs
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ANOC: an Asynchronous Network-on-Chip (1/2)

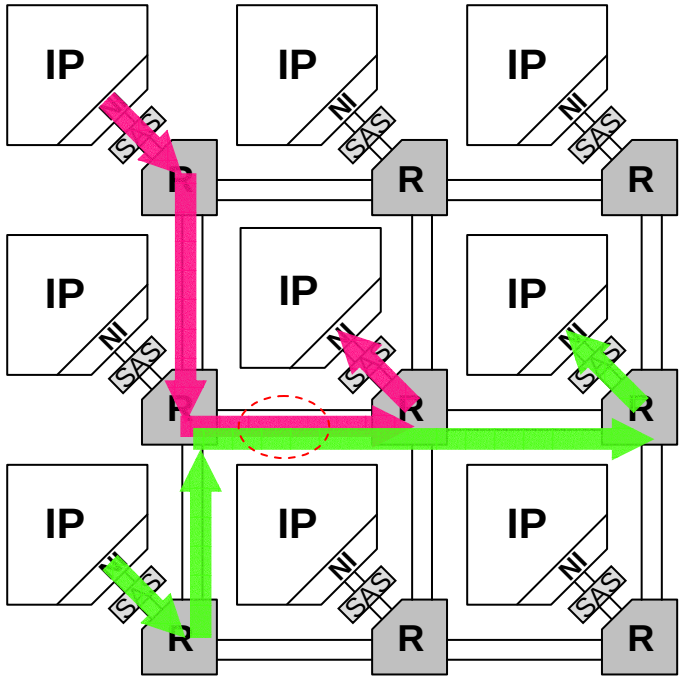
ANOC characteristics

- Wormhole, packet switching
- Implemented in asynchronous QDI logic

  QDI: Quasi Delay Insensitive
- 2 virtual channels

  SAS: Synchronous/Asynchronous Interface

  NI: Network Interface



Flit formats

BoP	EoP	Payload		*Path–to-Target*	
33	32	31	18	17	0

Header flit

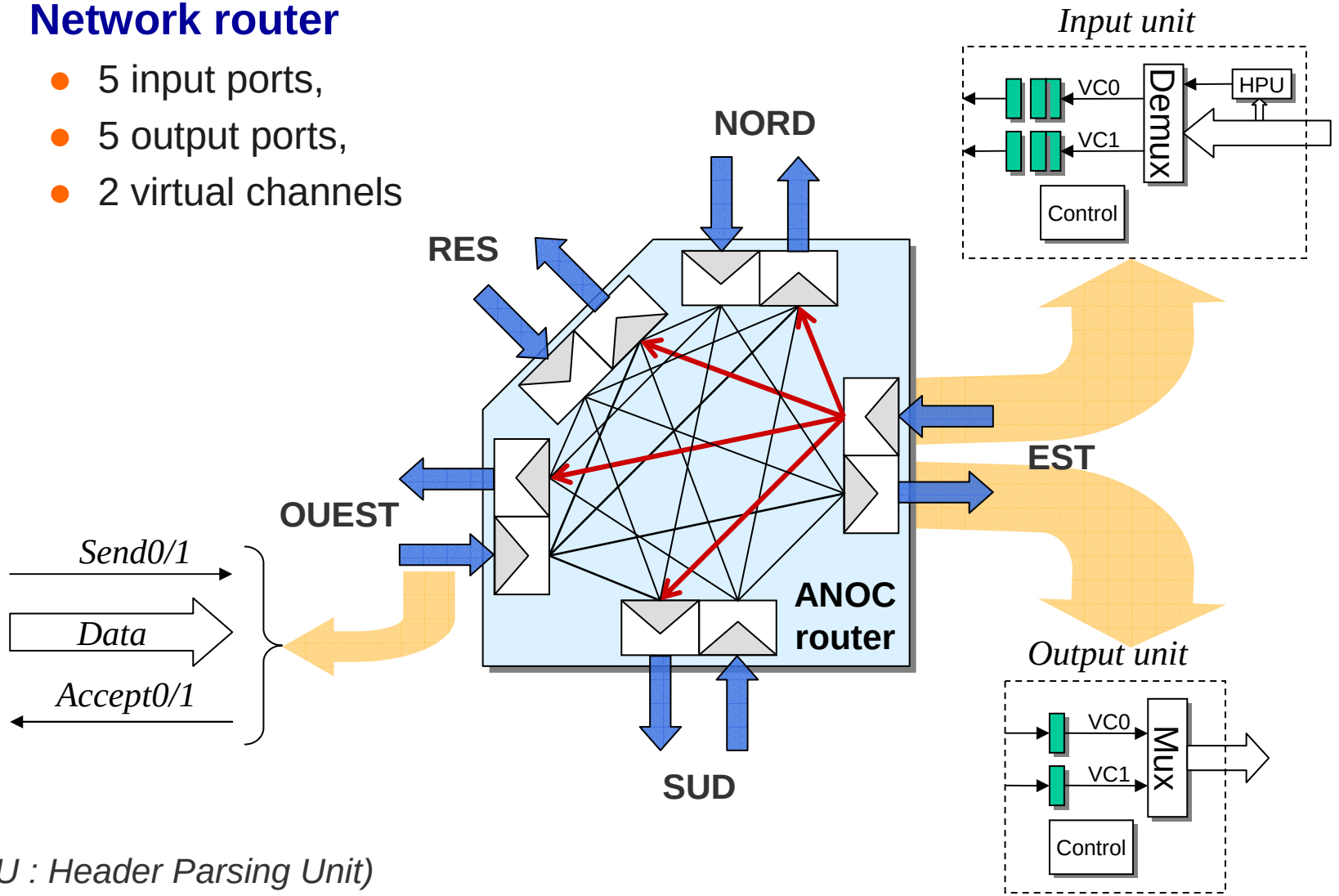
BoP	EoP	Payload	
33	32	31	0

Body flit or Tail flit

BoP	EoP	Type of flit
1	0	Header flit
0	0	Body flit
0	1	Tail flit
1	1	1-flit packet

ANOC: an Asynchronous Network-on-Chip (2/2)

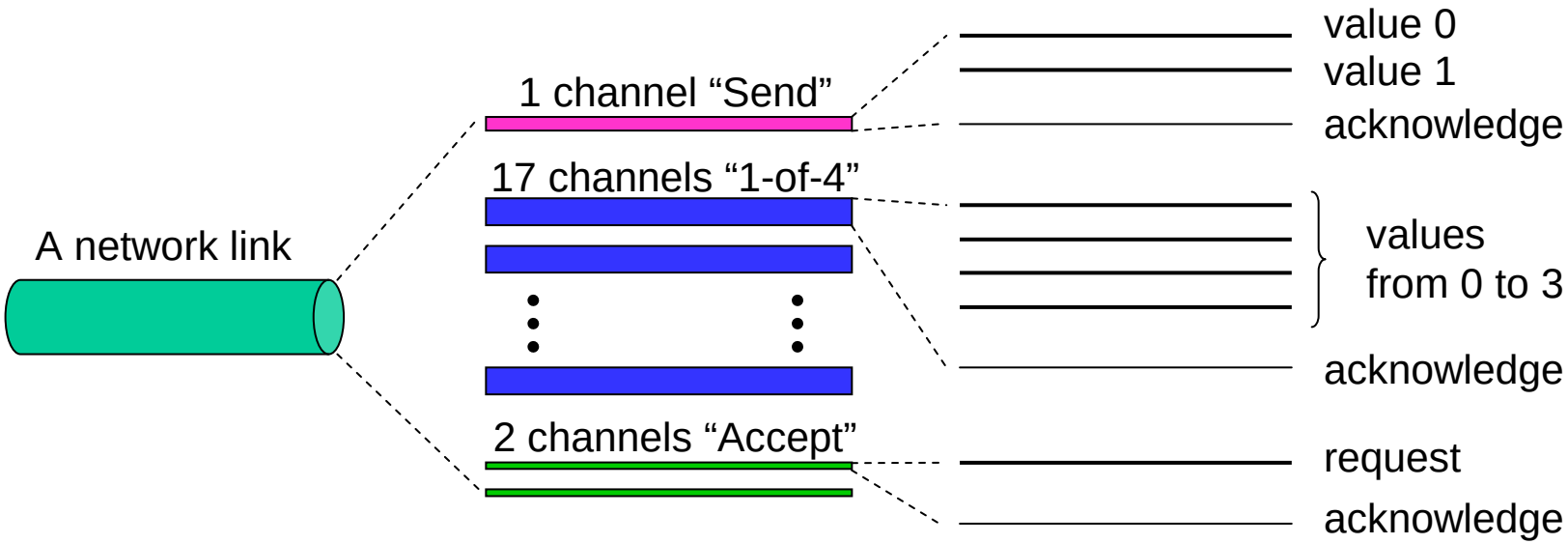
- **Network router**
  - 5 input ports,
  - 5 output ports,
  - 2 virtual channels



(HPU : Header Parsing Unit)

Test vectors generation (1/3)

- **Structure of network links**



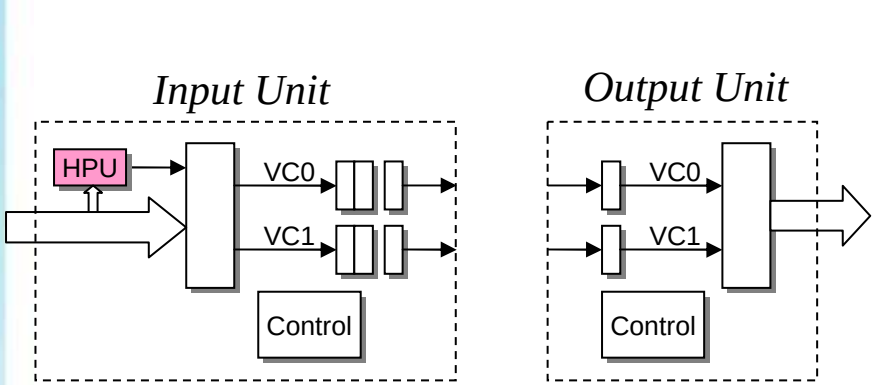
Data *(all 17 digits “1-of-4”)*	Send
« 0.0.0……0 »	« 0 »
« 1.1.1……1 »	« 1 »
« 2.2.2……2 »	« 0 »
« 3.3.3……3 »	« 1 »

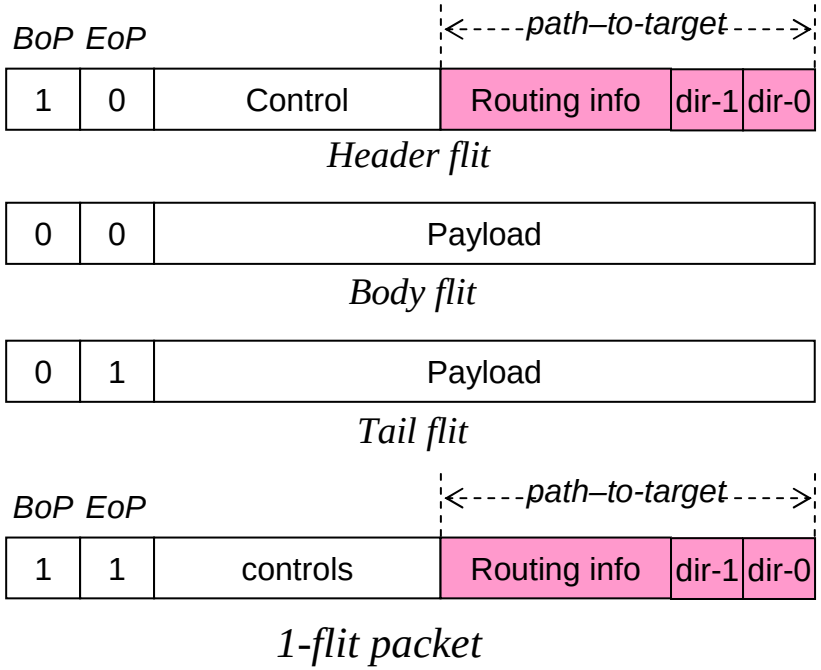
Total :

4 vectors

Test vectors generation (2/3)

Test vectors generation for network routers





Control information

- 4 outputs per input (“dir[dir-1,dir-0]” gets 4 possible values)
- 2 virtual channels (“vc” gets 2 possible values)
- Each router has 5 inputs: ➔ **x2 x 4 x5 values for dir and vc**
- BoP/EoP (= 0/1 → no-shifting path, = 2/3 → shifting path)

4 possible values of payload

4 possible values of payload

Test vectors generation (3/3)

Test vectors generation for network routers

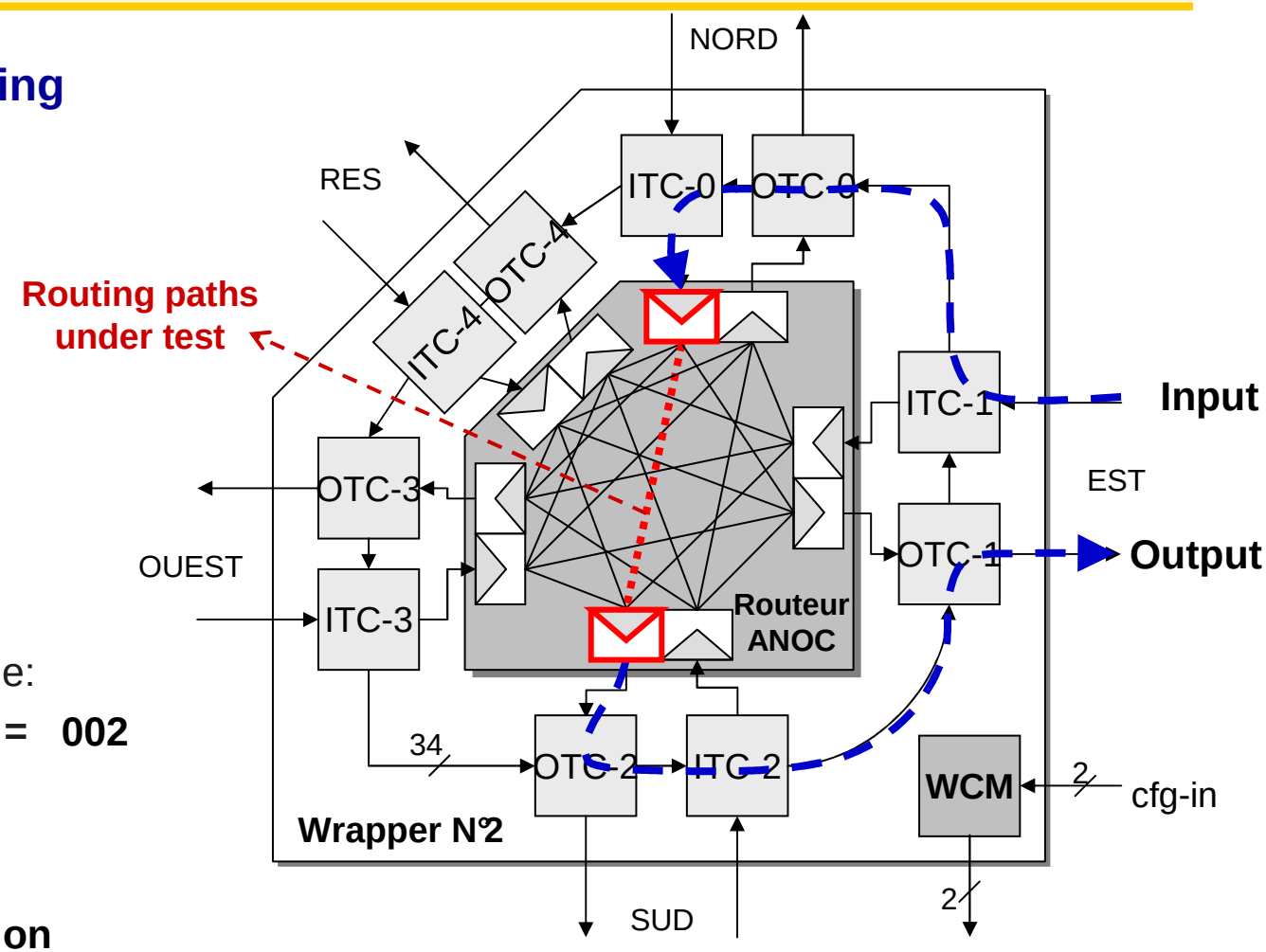
- Test vectors for a triplet “input/output/virtual channel”

Data			Send
BoP/EoP	15 digits « 1-of-4 »	direction	channel
« 2 »	« 0.0.0……0 »	« dir. »	« vc. »
« 0 »	« 0.0.0……0 »	« 0 »	« vc. »
« 0 »	« 1.1.1……1 »	« 1 »	« vc. »
« 0 »	« 2.2.2……2 »	« 2 »	« vc. »
« 1 »	« 3.3.3……3 »	« 3 »	« vc. »
« 3 »	« 1.1.1……1 »	« dir. »	« vc. »
« 3 »	« 2.2.2……2 »	« dir. »	« vc. »
« 3 »	« 3.3.3……3 »	« dir. »	« vc. »

<u>Total:</u> 5 inputs x 4 outputs per input x 2 virtual channels x 8 vectors
= 320 test vectors (for a router)

Application of the test vectors (1/2)

- **Routers testing**



- An example:
  Router ID = 002

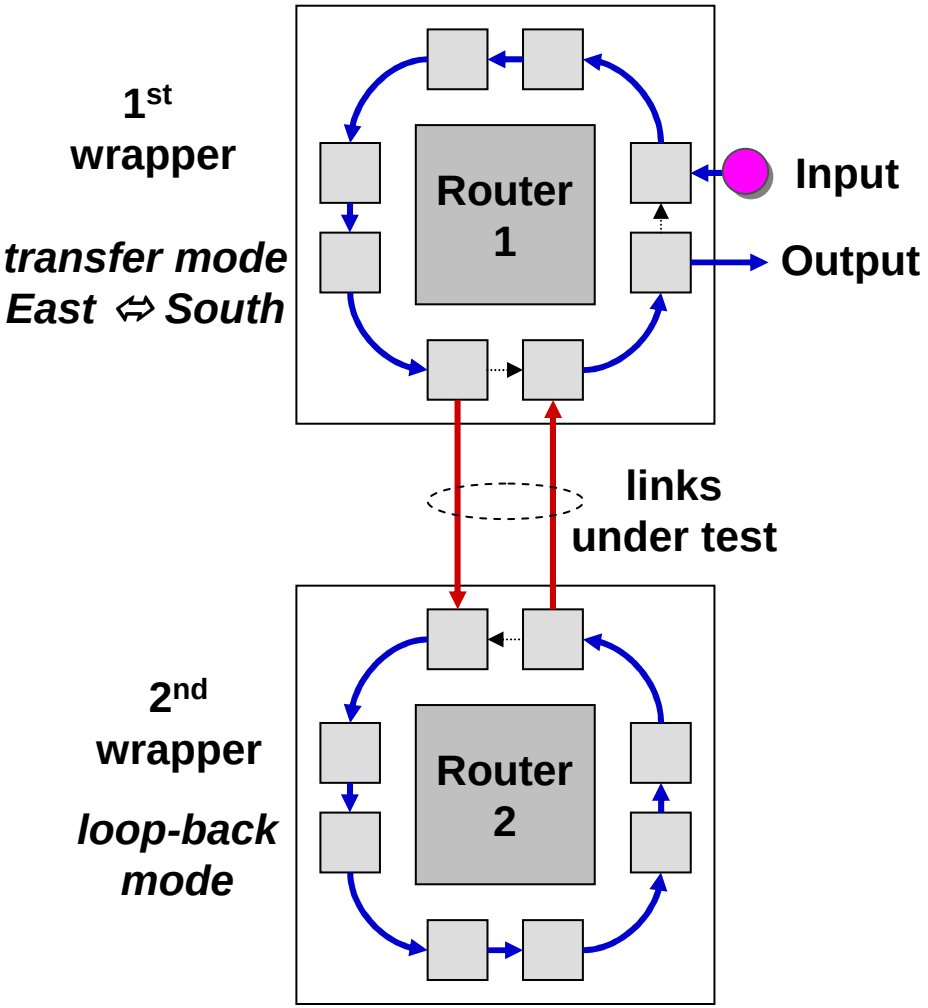
Test configuration

EoF	ID	$R_S - R_E$	$O_S - O_E$	$S_S - S_E$	$E_S - E_E$	$N_S - N_E$	M
3	002	00 – 00	00 – 00	01 – 02	12 – 01	02 – 12	1

Application of the test vectors (2/2)

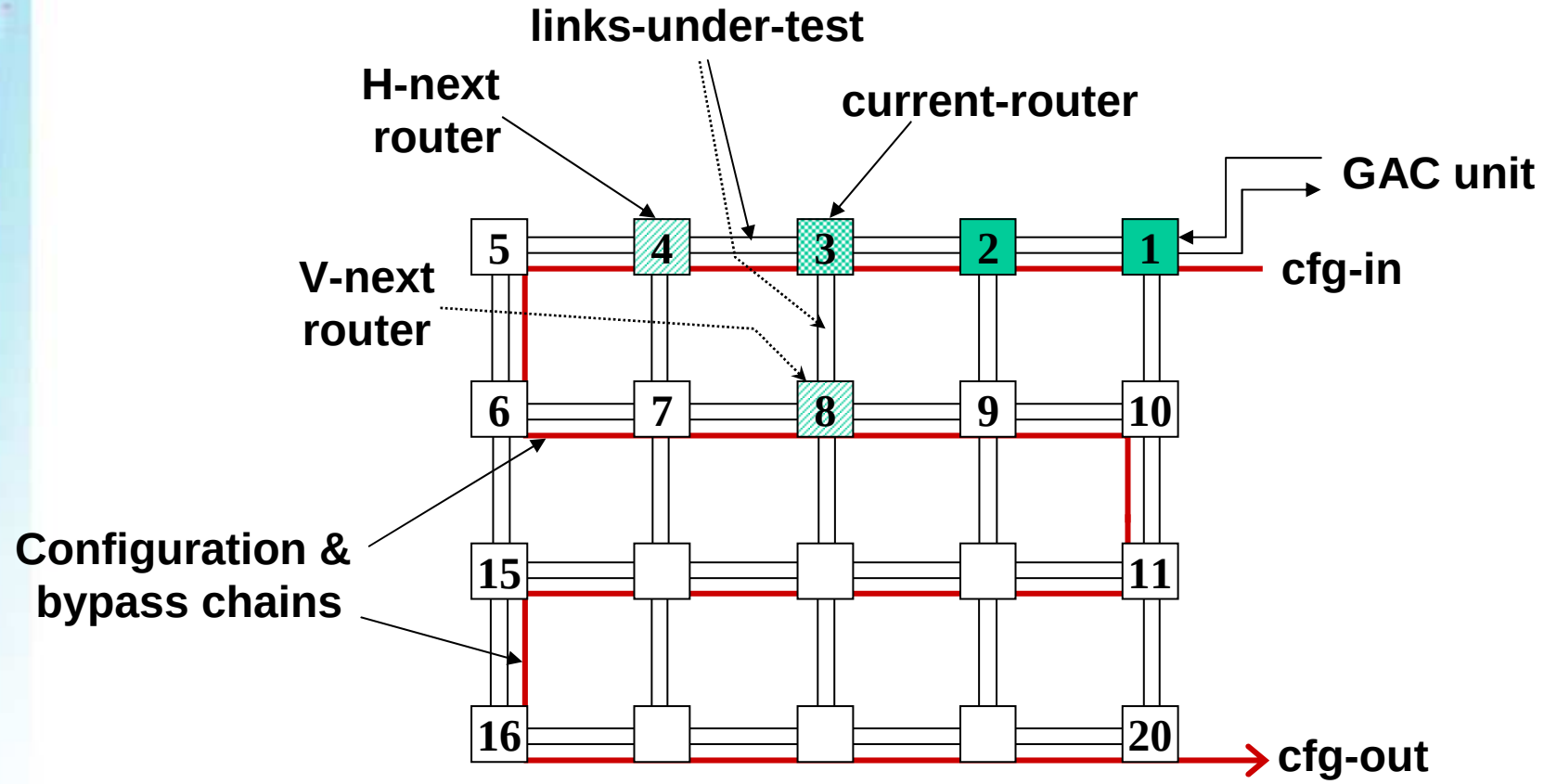
Network links testing

- 2 wrappers are used
- 2 test configurations
- 2 network links are tested at the same time



Testing algorithm for the entire network

- **Global testing strategy**



- *Note:* already tested routers are put in bypass mode

Test results (1/3)

Test application time

- Test speed: 10M-vecteurs/s

Size of network under test	Test application time (µs)		
	routers	*network links*	*entire network*
1 x 1	**32**		
3 x 3	**288,40**	**5,20**	**293,20**
3 x 4	**384,55**	**7,35**	**391,35**
4 x 4	**512,75**	**10,35**	**522,35**
5 x 4	**640,95**	**13,35**	**653,35**

- For the considered size, test application time is less than 1*ms* (less than the test application time of an IP used in our system)

Test results (2/3)

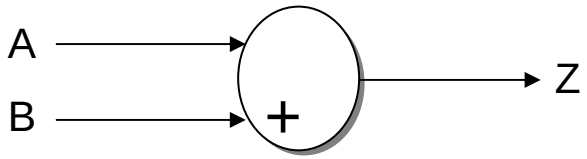
Fault coverage (the test of network architecture)

- Fault coverage for network links testing: 100%
- Fault coverage for routers testing:

Circuit under test	Input unit	Output unit	Entire router
SSAF on both inputs and outputs	9194/9194 **(100%)**	14110/14142 **(99,77%)**	116520/116680 **(99,86%)**

Undetected faults

- Inputs of a few asymmetric C-elements



- Does not consider the level 0 on entry B
- Unable to verify the stuck-at-1 on B, the transition on Z can happen too soon

Test results (3/3)

Fault coverage (the test of the proposed DfT architecture)

Circuit under test	Test cell	WCM	Entire wrapper
SSAF on both inputs & outputs	3380/3382 (99,94%)	3400/3472 (97,93%)	**37200/37292 (99,75%)**

Undetected faults

- On the signals concerned to the ID verification of test wrapper,
- On the control signals ‘ctrl-mode’ of test cells (inputs of a few asymmetric C-elements)

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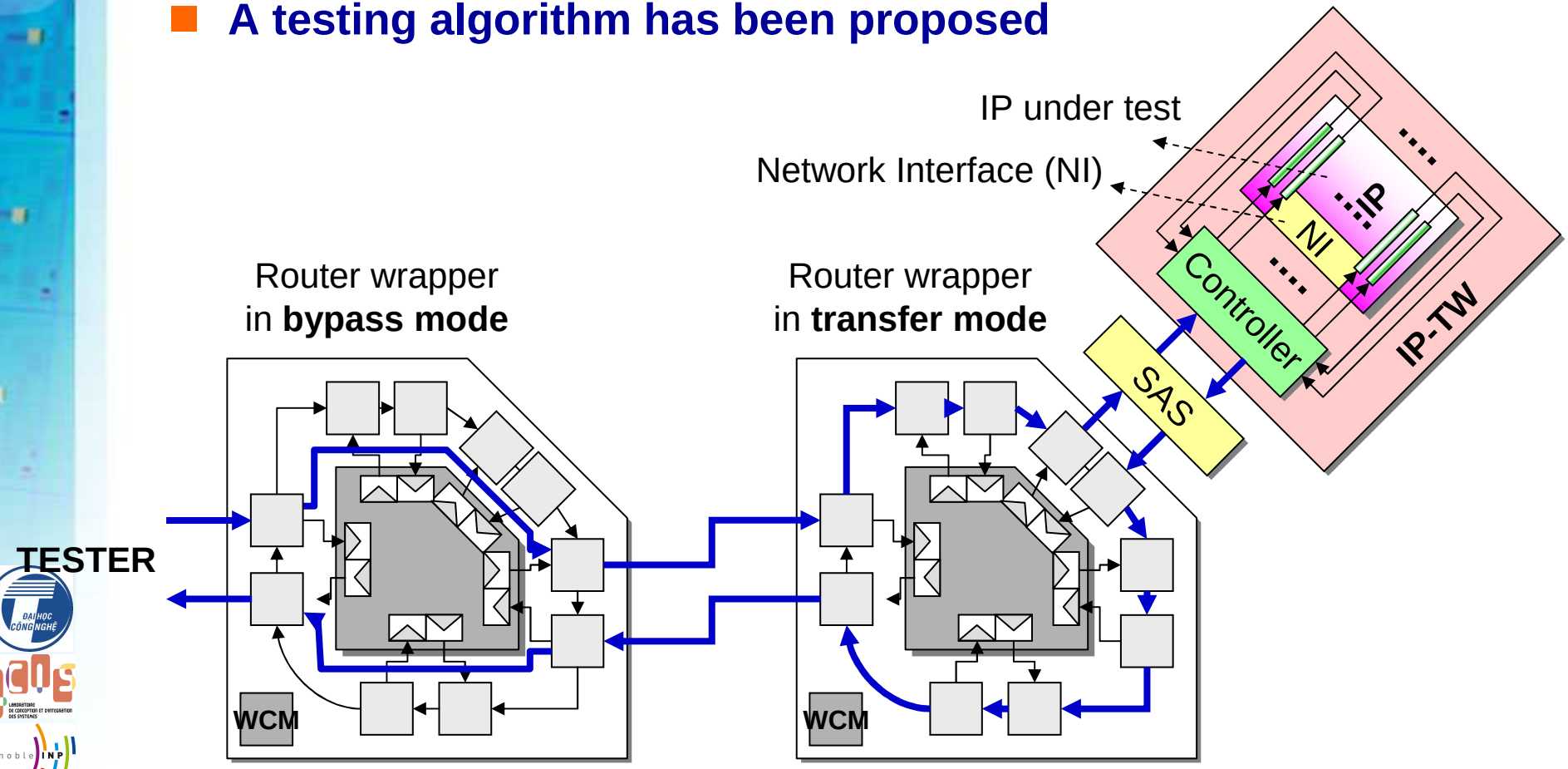
IP cores testing with the proposed DfT architecture

- **The proposed DfT architecture is used as a TAM**
- **Scan chains are configured and read from the TAM**
- **A testing algorithm has been proposed**



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Conclusions

- **Design and Implementation of an asynchronous DfT architecture for asynchronous NoCs with different topologies**
  - Design & implementation
  - Integration to a test chip
  - Small added latency
  - No bandwidth degradation

- **Application to the ANOC network**
  - Test vectors generation, testing algorithm, test results evaluation (fault coverage, test application time, etc.)
  - Faulty routers can be isolated by test wrapper

- **Reuse of the DfT architecture for other alternative uses**
  - **IP testing**, *Verification, Debug (not presented in this talk)*

Perspectives

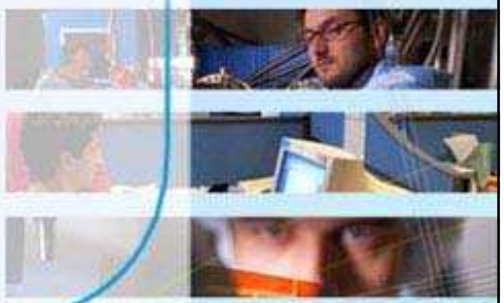
- **Validate the physical implementation of the proposed DfT architecture on the ALPIN test chip (in progress)**
- **Optimize the test application time for the IPs testing, considering additional surface cost constraints**
  - Configure in parallel the test wrappers
  - Add reconfigurable bypasses
- **Implement an on-chip GAC unit in order to realize an auto-testable Network-on-Chip**
  - Very important for industrial transfer
  - BIST (Built-In Self-Test) of asynchronous networks

micro and nanoelectronics
microsystem
ambient intelligence
biology and health
image chain

Innovation for industry

Thank You !

Loyalty
Entrepreneurship
Team work
Innovation



VNU-COLTECH: College of Technology, Vietnam National University, Hanoi