Coping with Soft Errors in Asynchronous Burst-Mode Machines

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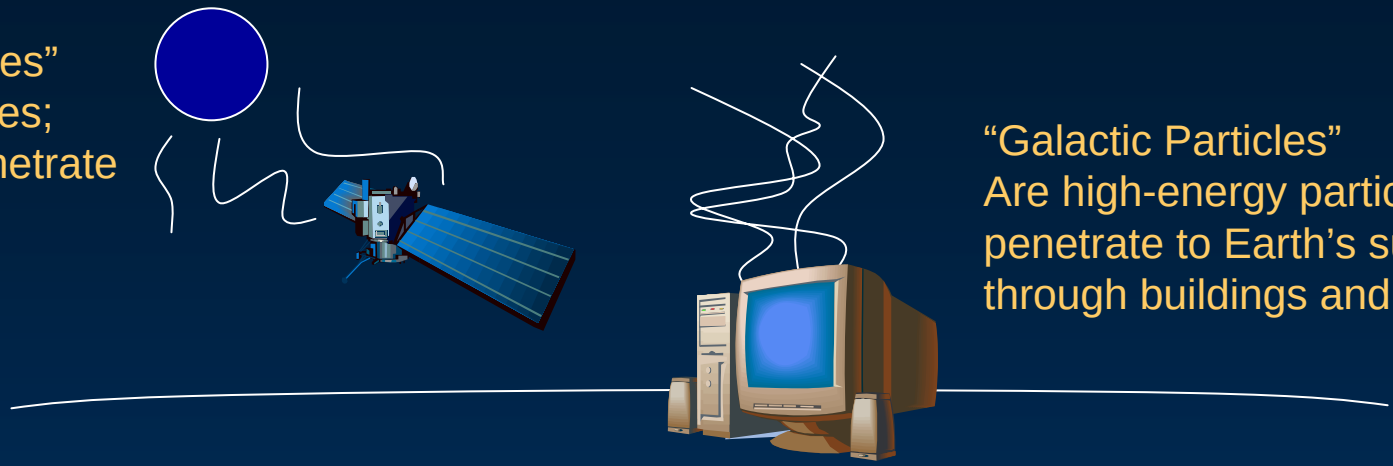
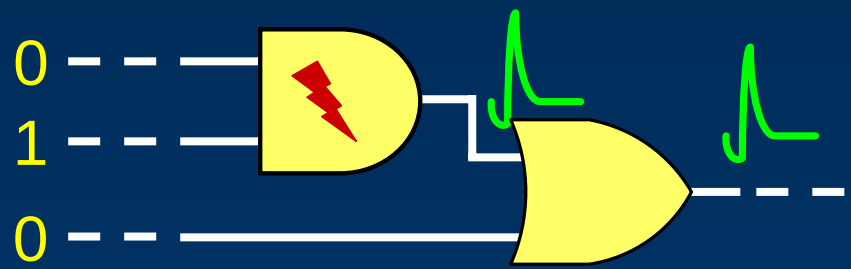
Sources of Soft Errors

"Solar Particles"
Affect satellites;
may also penetrate
to Earth



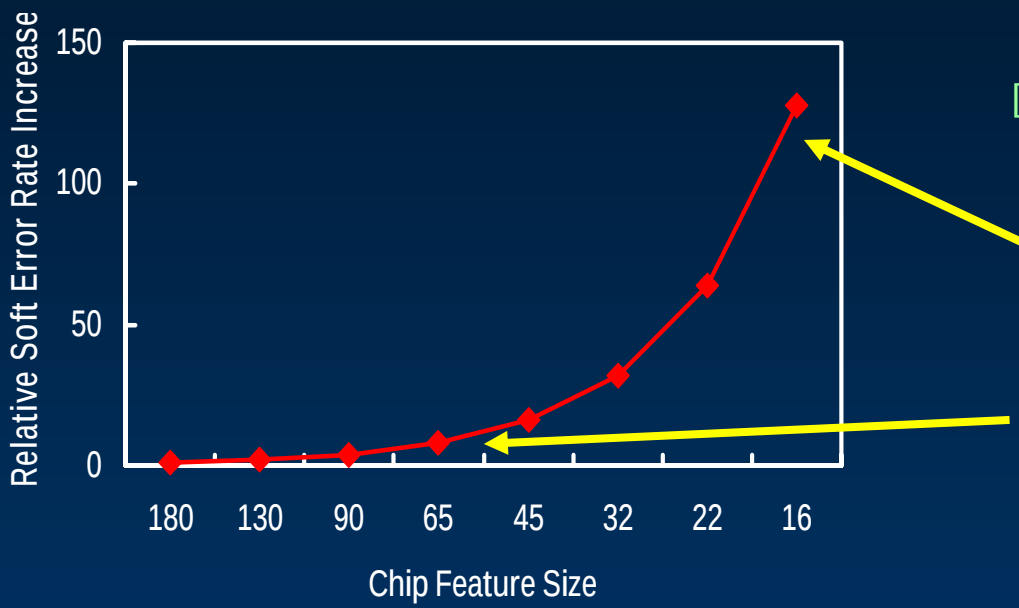
"Galactic Particles"
Are high-energy particles that
penetrate to Earth's surface,
through buildings and walls

- High-energy particles collide with silicon atoms
- Collision generates a voltage pulse at impact site



- Under certain conditions, it may produce a soft error

Frequency of Soft Errors



Soft Error Rate Trends
[S. Borkar et al., Intel, DAC'04]

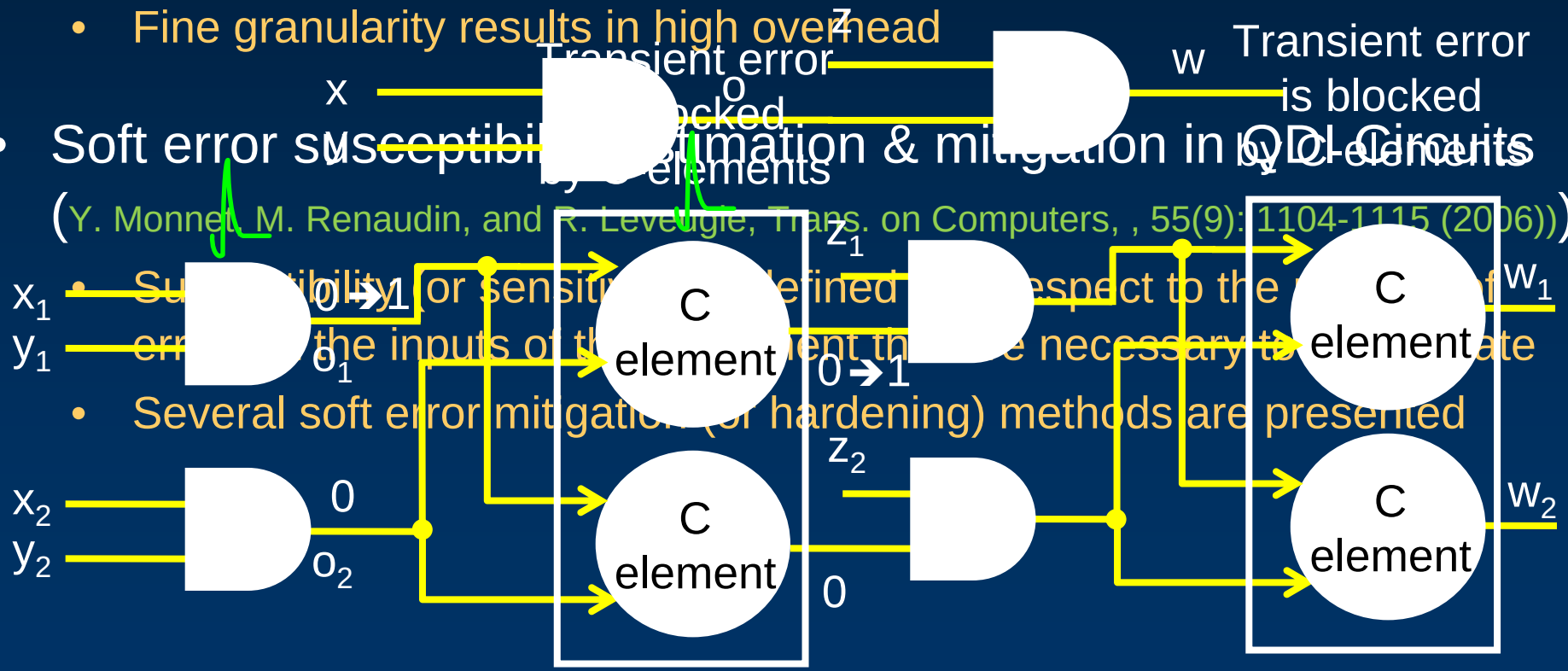
6 years
from now

we are
approximately
here

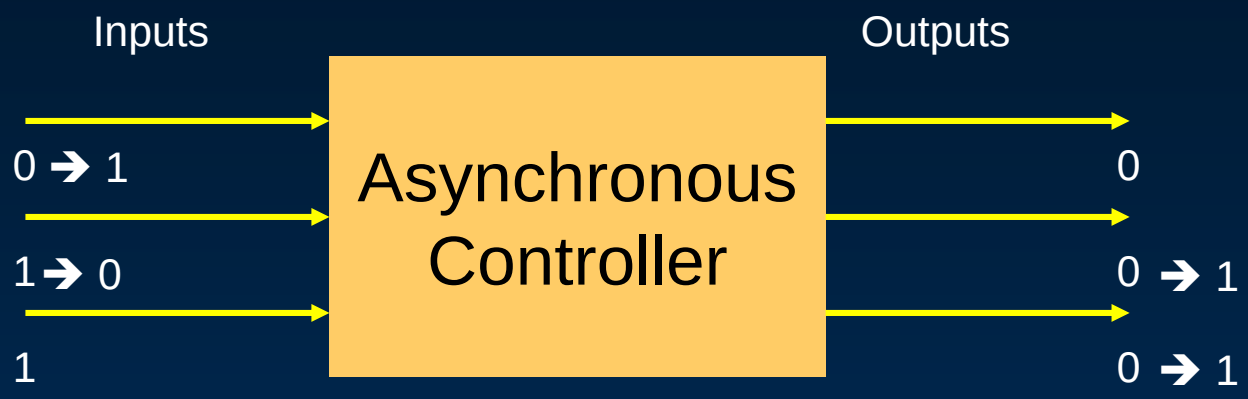
- Integrated circuits (synchronous & asynchronous) will require methods to tolerate / mitigate soft errors and ensure reliability

Soft Error Tolerance & Mitigation in ASYNC

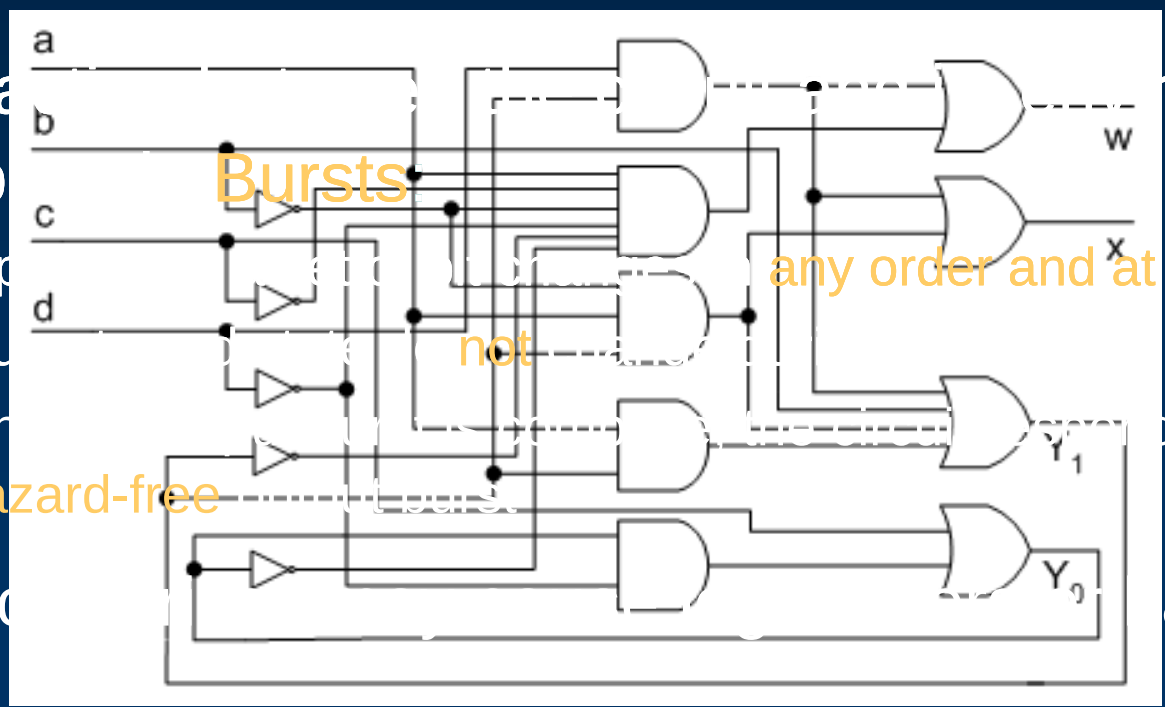
- Previous studies targeted Quasi Delay-Insensitive (QDI) circuits
- SEU-tolerant QDI circuits (W. Jang & A. Martin, ASYNC, 156-165, 2005):
  - Gate-level fine-grain duplication and double-checking
  - Fine granularity results in high overhead
- Soft error susceptibility estimation & mitigation in QDI Circuits (Y. Monnet, M. Renaudin, and R. Leveugle, Trans. on Computers, , 55(9): 1104-1115 (2006)):
  - Susceptibility (or sensitivity) defined with respect to the number of erroneous inputs of the gate sufficient that are necessary to propagate
  - Several soft error mitigation (or hardening) methods are presented



Asynchronous Burst-Mode Machines

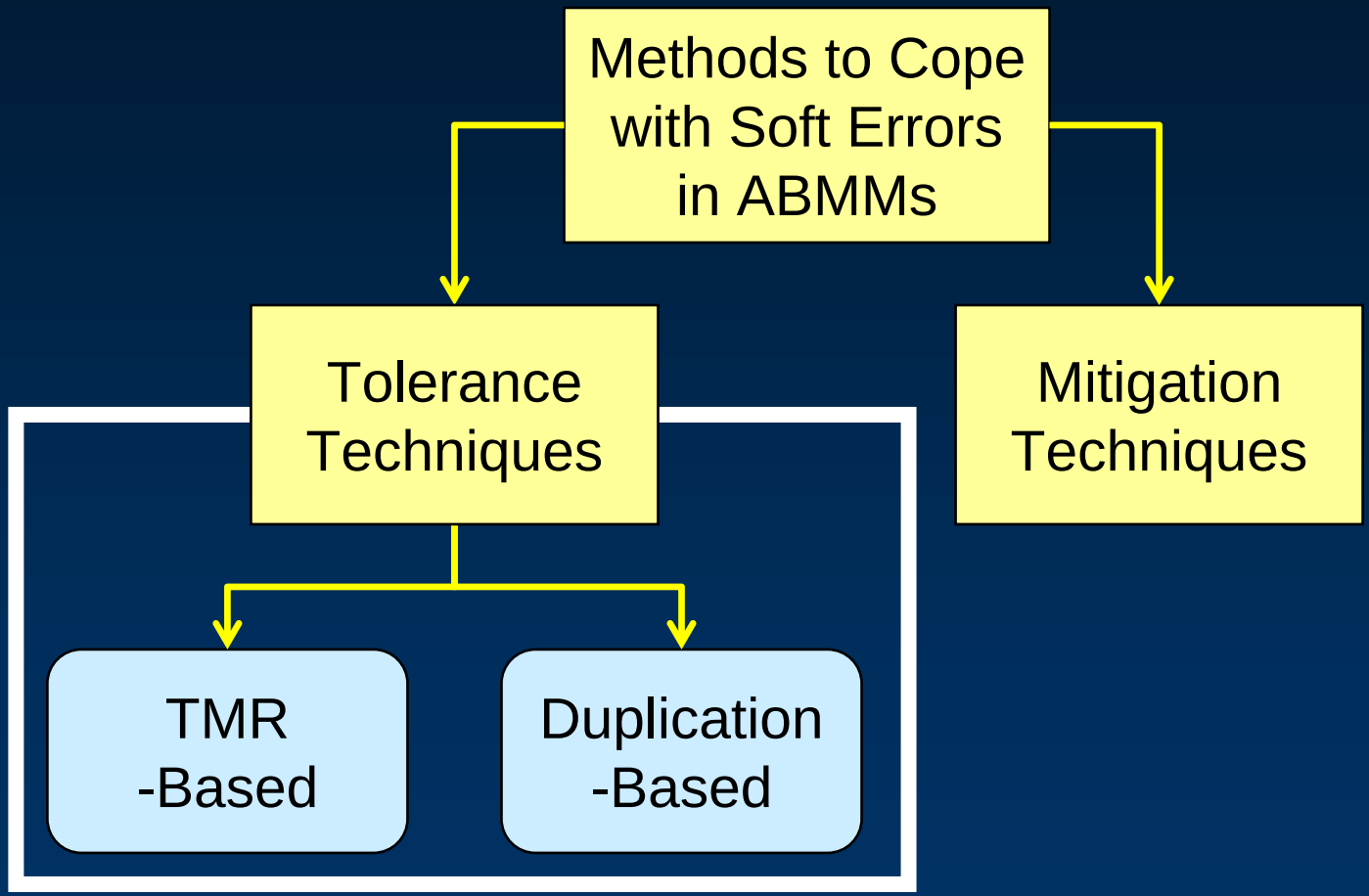


- Intera… …ronment happ…
  - Inp… …any order and at any time
  - Ou… …rst
  - On… …ds with a hazard-free …
- Partic… …azards

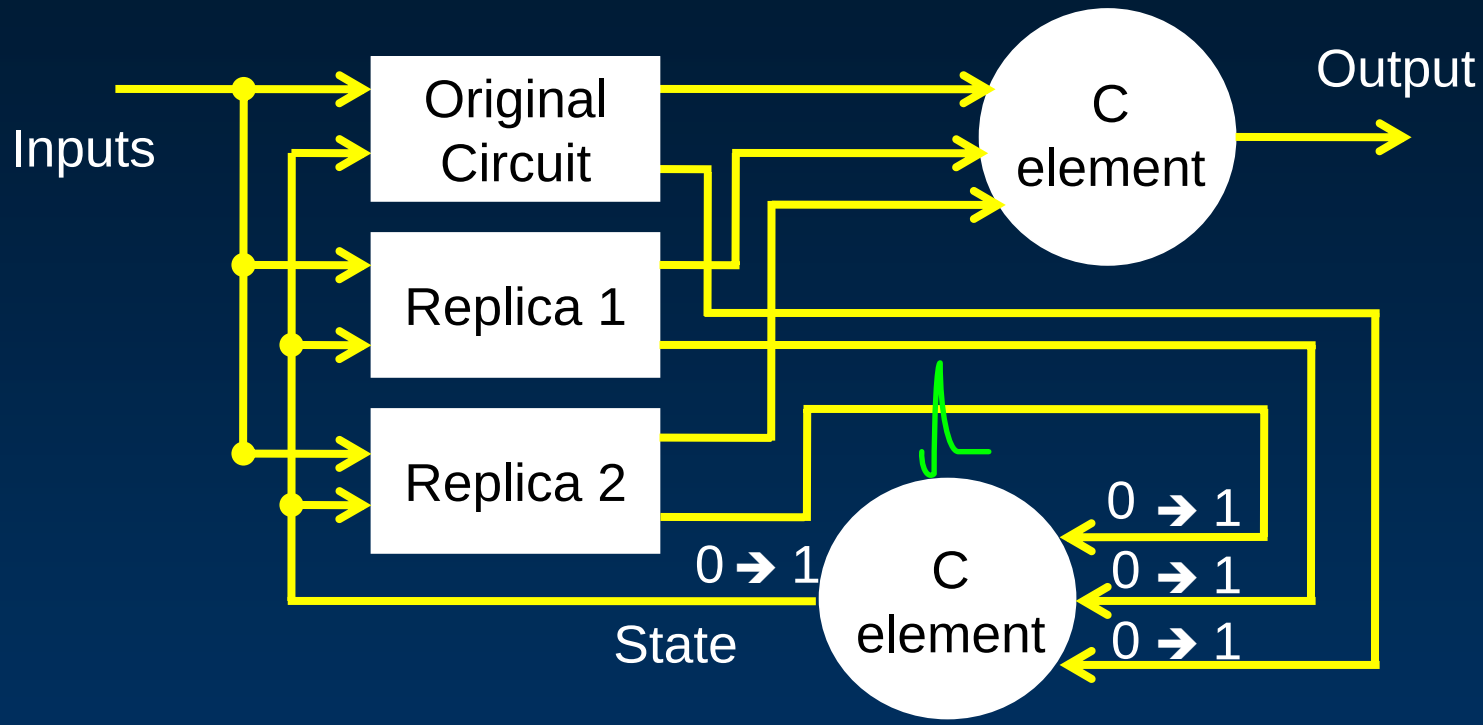


Bursts

Coping with Soft Errors in ABMMs



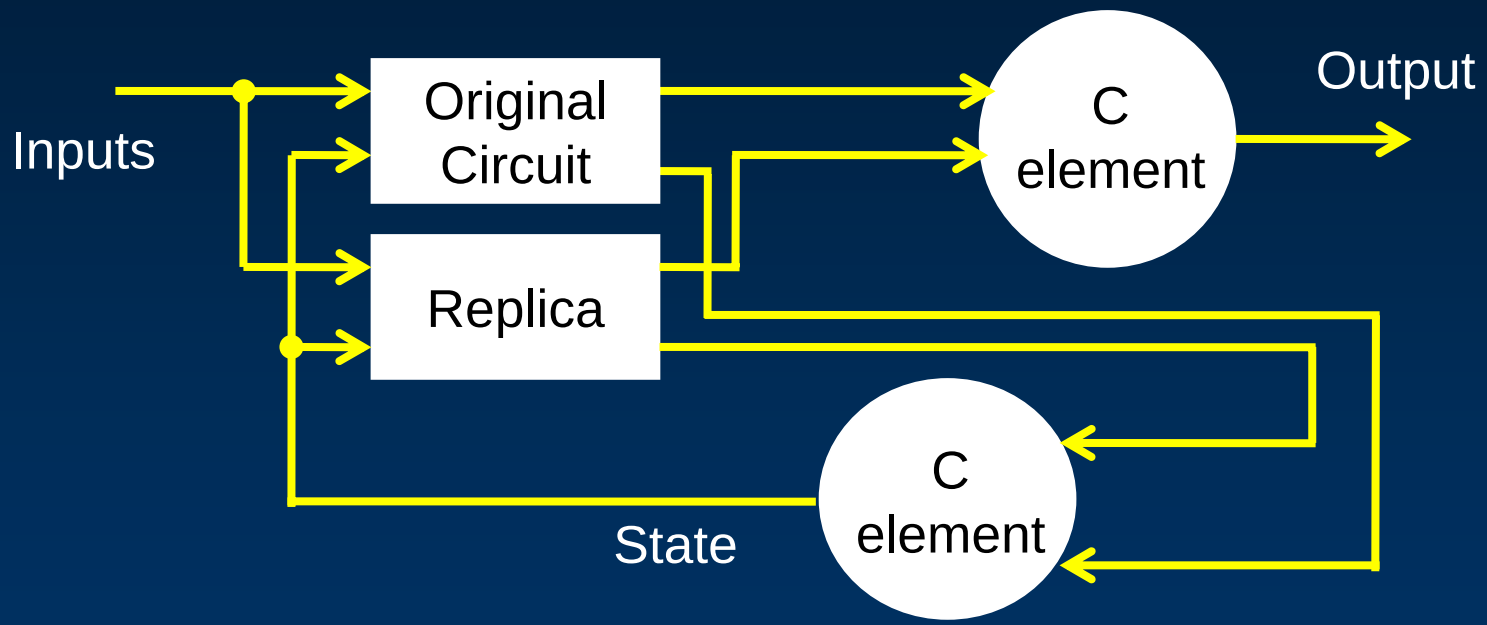
TMR-based Soft Error Tolerance in ABMMs



- C-element used as majority voter
- Strikes at state-line C-elements not tolerated

Duplication-based Soft Error Tolerance

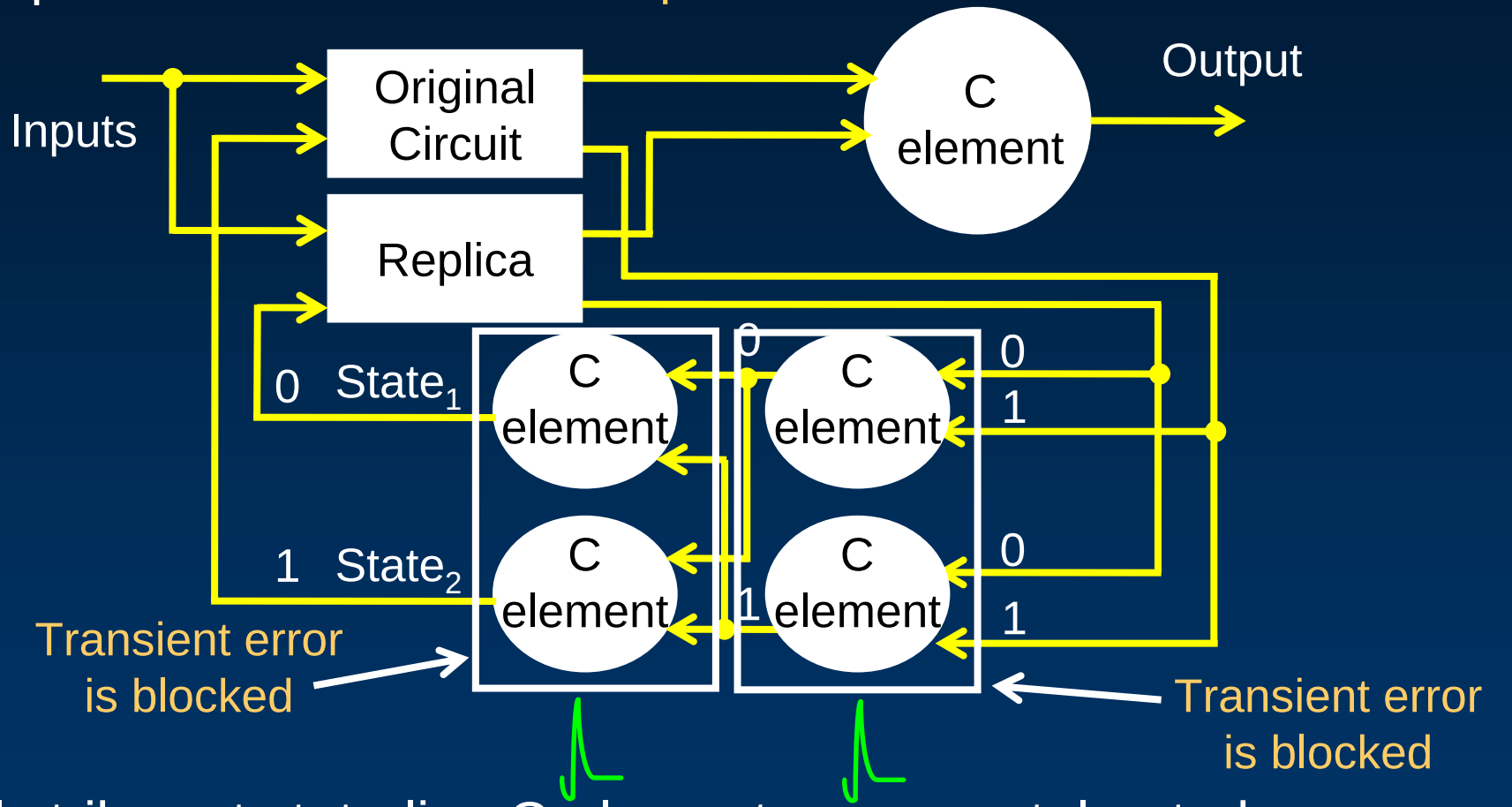
- Observation: 2-input C-elements are sufficient to tolerate one failing module (i.e., only one replica is needed)



- Strikes at state-line C-elements still not tolerated

Tolerating Errors on State-Line C-Elements

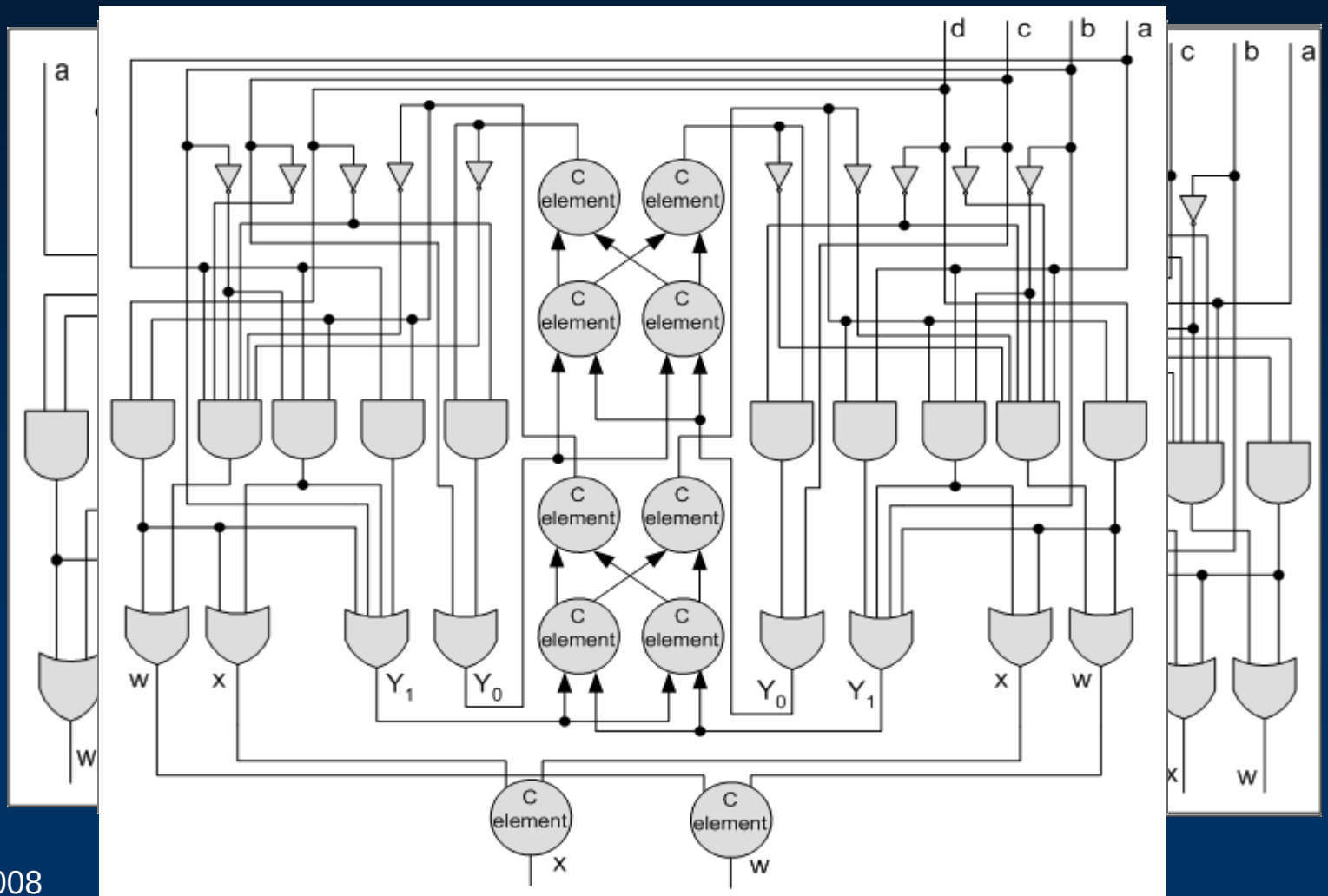
- Proposed Solution: cross-coupled structure of C-elements



- All strikes at state-line C-elements are now tolerated

Example

3. Insert state-holding elements



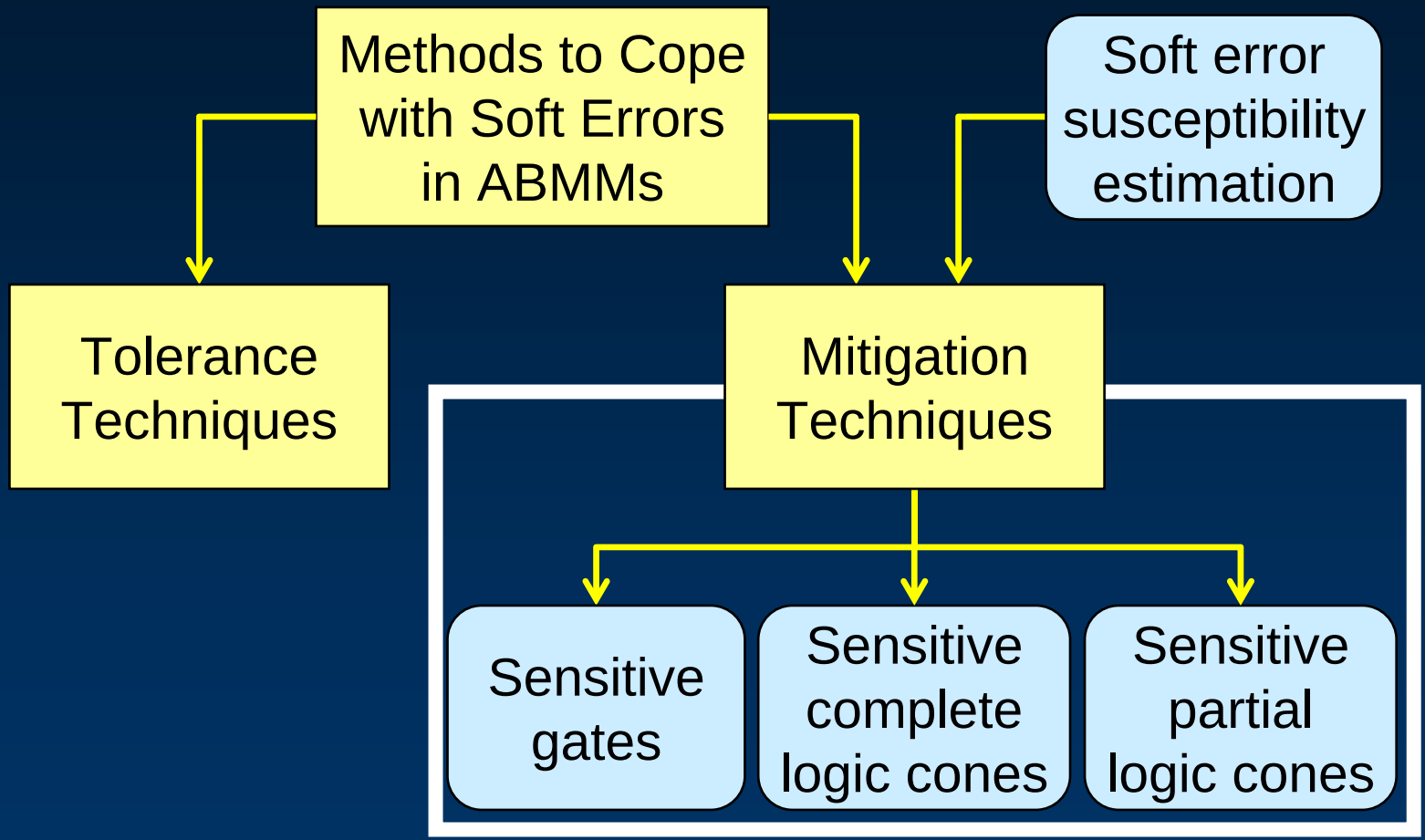
Experimental Results

Duplication-based Soft Error Tolerance

Circuit Name	I/S/O	Original	Duplicate	C-elements	Total	Overhead
hp-ir	3/1/2	8	8	18	34	325.00%
concur-mixer	3/2/3	16	16	33	65	306.25%
tangram-mixer	3/1/2	10	10	18	38	280.00%
rf-control	6/3/5	37	37	51	125	237.84%
while_concur	4/2/3	24	24	33	81	237.50%
barcode	13/4/17	172	172	99	443	157.56%
p2	8/4/16	192	192	96	480	150.00%
p1	13/4/14	238	238	90	566	137.82%

Area overhead seems excessive for small circuits: cost inflated due to proportionately large number of C-elements over logic gates, and the rather expensive C-element implementation used

Coping with Soft Errors in ABMMs



Soft Error Susceptibility Estimation

- A hazard-aware asynchronous fault simulator is needed

(SPIN-SIM: F. Shi and Y. Makris, ITC, 597-606 (2004))

- Fault simulate & construct a *soft error susceptibility table* (*sest*)
- Asymmetric soft error susceptibility of gates in different levels
  - Enables judicious selection and replication in a *partial duplicate*

(K. Mohanram and N. A. Touba, ITC, 893-901 (2003))

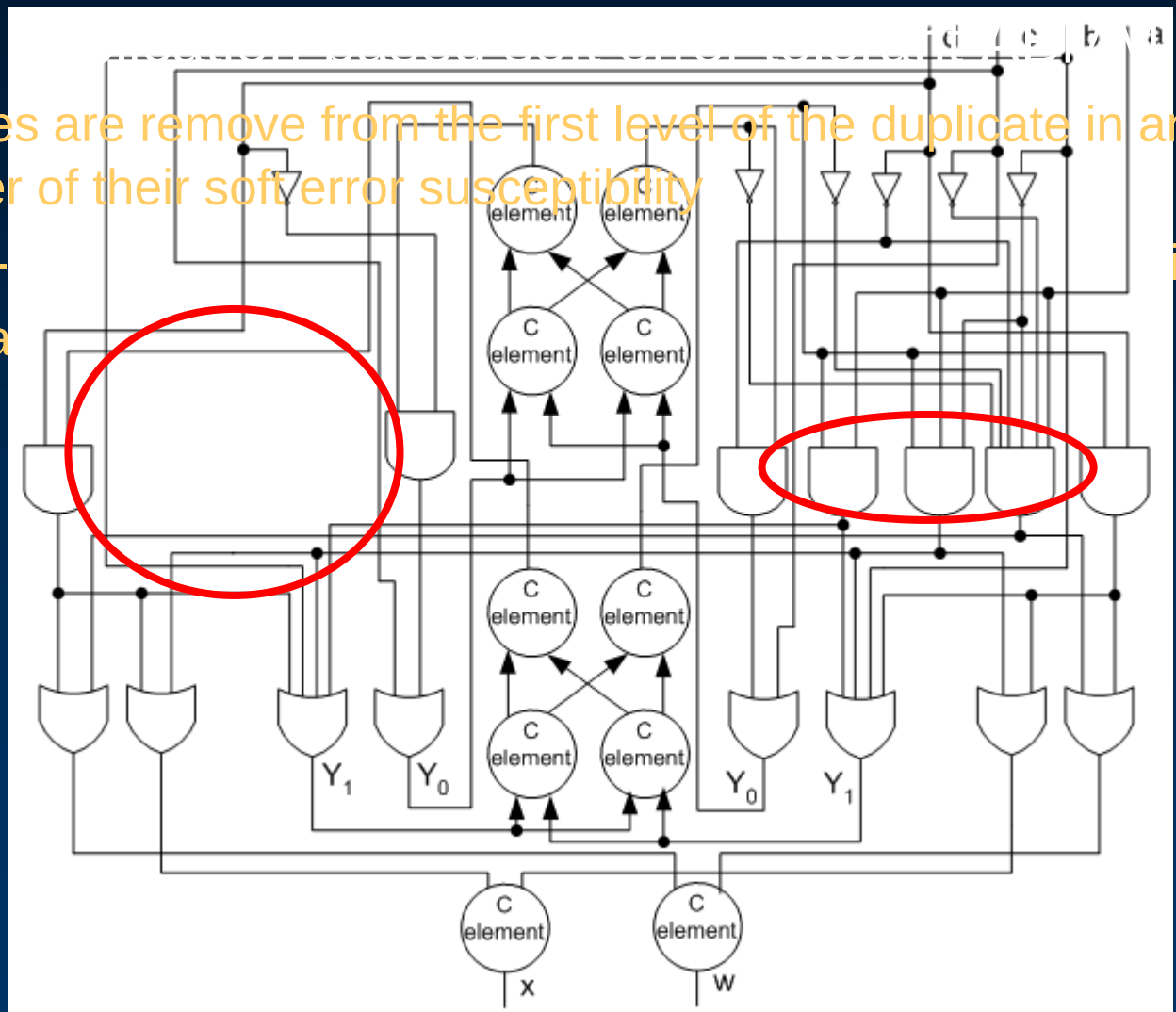
State & Input Burst Pair	Potential SETs			
	f_1	f_2	..	f_n
SIB_1	11000	00000	..	00001
SIB_2	01001	11001	..	11001
.	..	..	..	..
SIB_m	11001	00010	..	00000

$$susc(G_q) = \frac{\sum_{i=1}^{m} \sum_{j=s+1}^{s+k_q} E(sest[i,j])}{m \,.\, k_q}, \text{ where } s = \sum_{l=1}^{q-1} k_l$$

$$SER(ABMM) = \sum_{q=1}^{n} sest(G_q)$$

Duplication of Sensitive Gates

- Using a
  1. Gates are remove from the first level of the duplicate in an increasing order of their soft error susceptibility
  2. Fan- inal ABMM
  3. Area

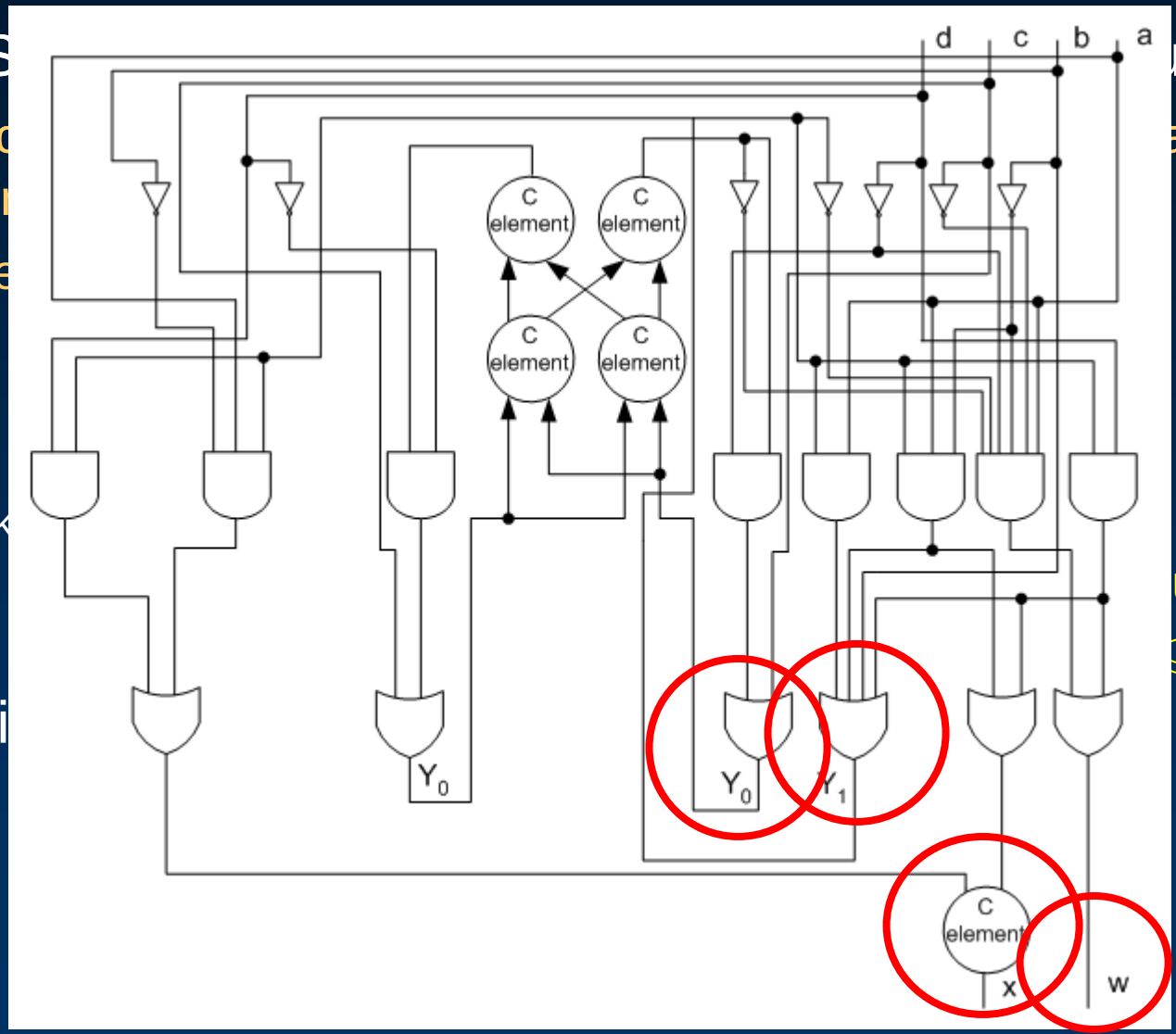


Cost:
87% Gates removed
Tolerance:
68%

Drives fan-outs of removed gates

Duplication of Complete Sensitive Logic Cones

- Output/S… …usceptibility:
  - Selec… …ation
  - maxi…
  - Mode…



Cost:

60% Tol(Y_k…

Tolerance :

47% Maximi…

(i) C_k <…

(ii) X_s ϵ …

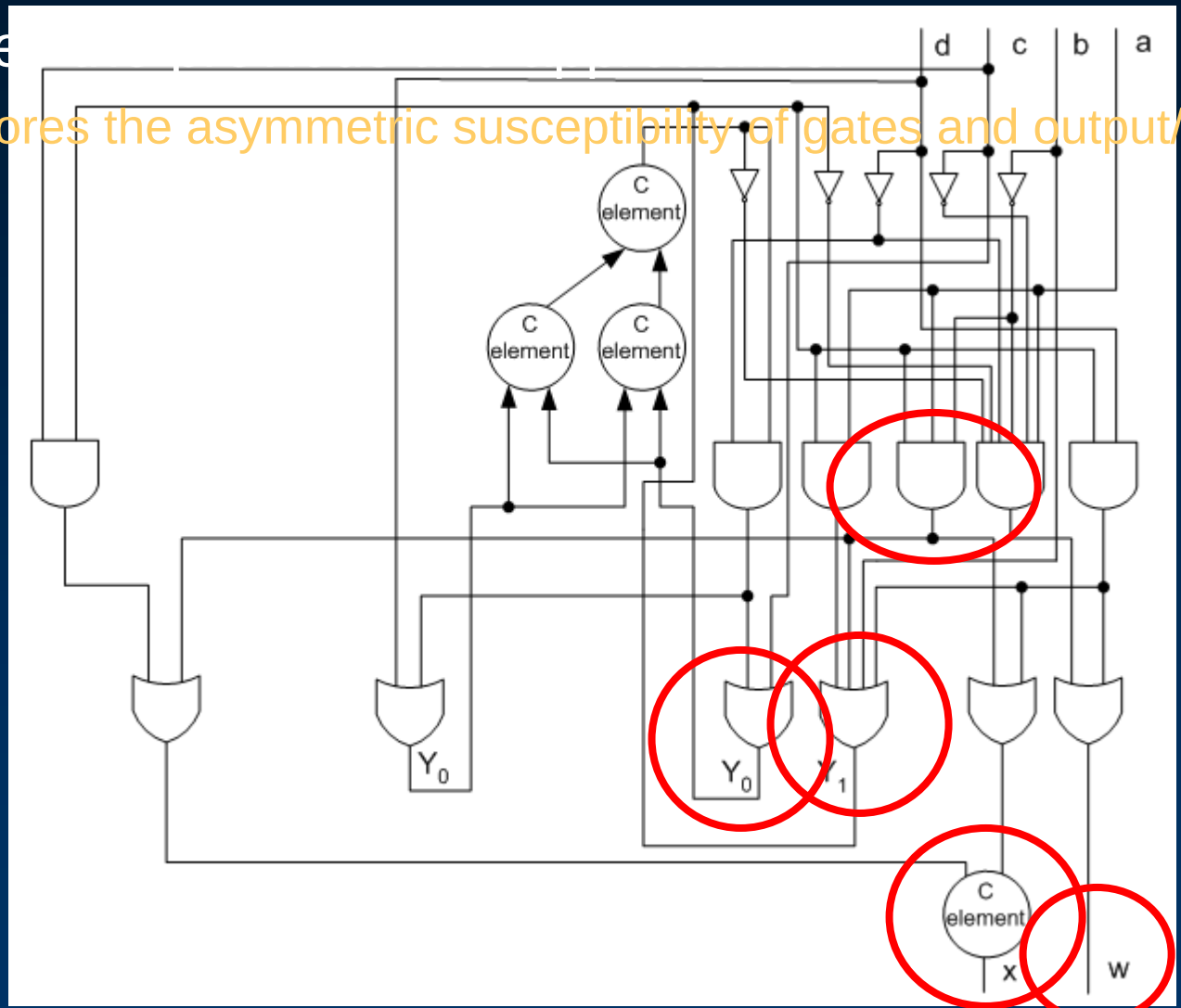
…utput lines

…Y_0 & w not protected

…protected complete protection

Duplication of Partial Sensitive Logic Cones

- Combine
  - Explores the asymmetric susceptibility of gates and output/state lines



Cost:
50%

Tolerance:
24%

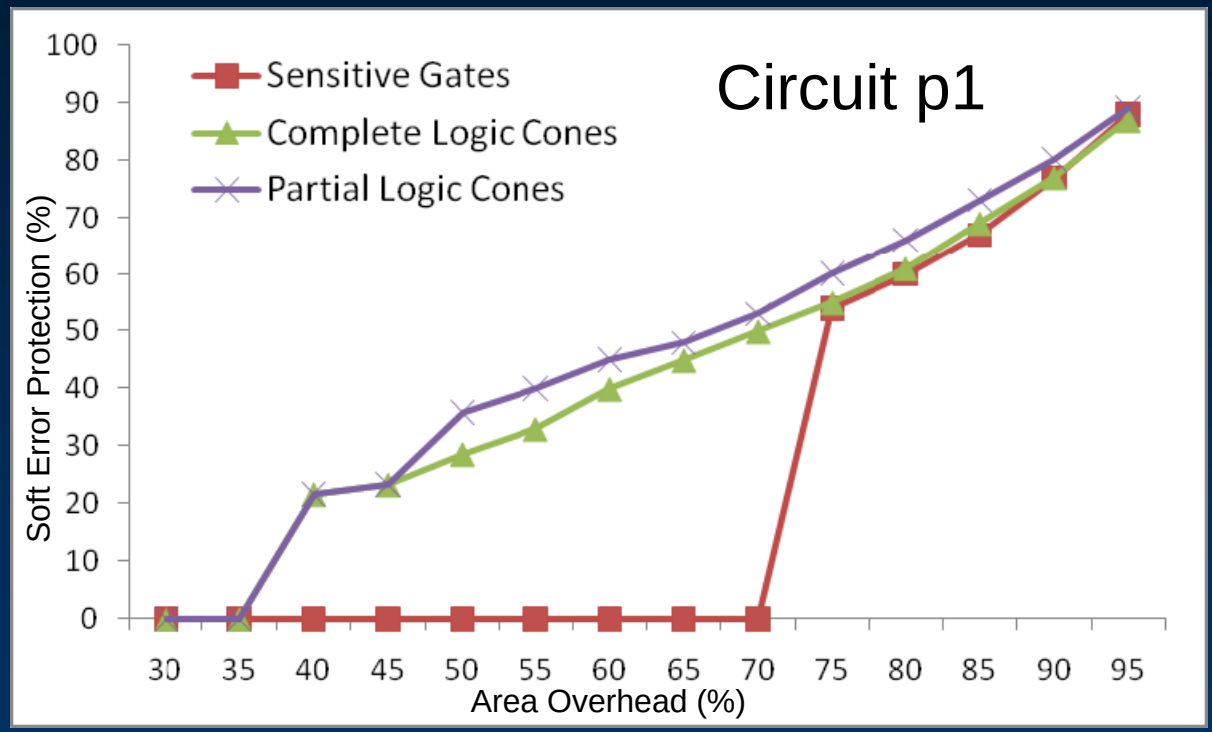
Drives fan-out of removed gate

Y and x not protected

partial protection

Experimental Results

2-level ABMMs



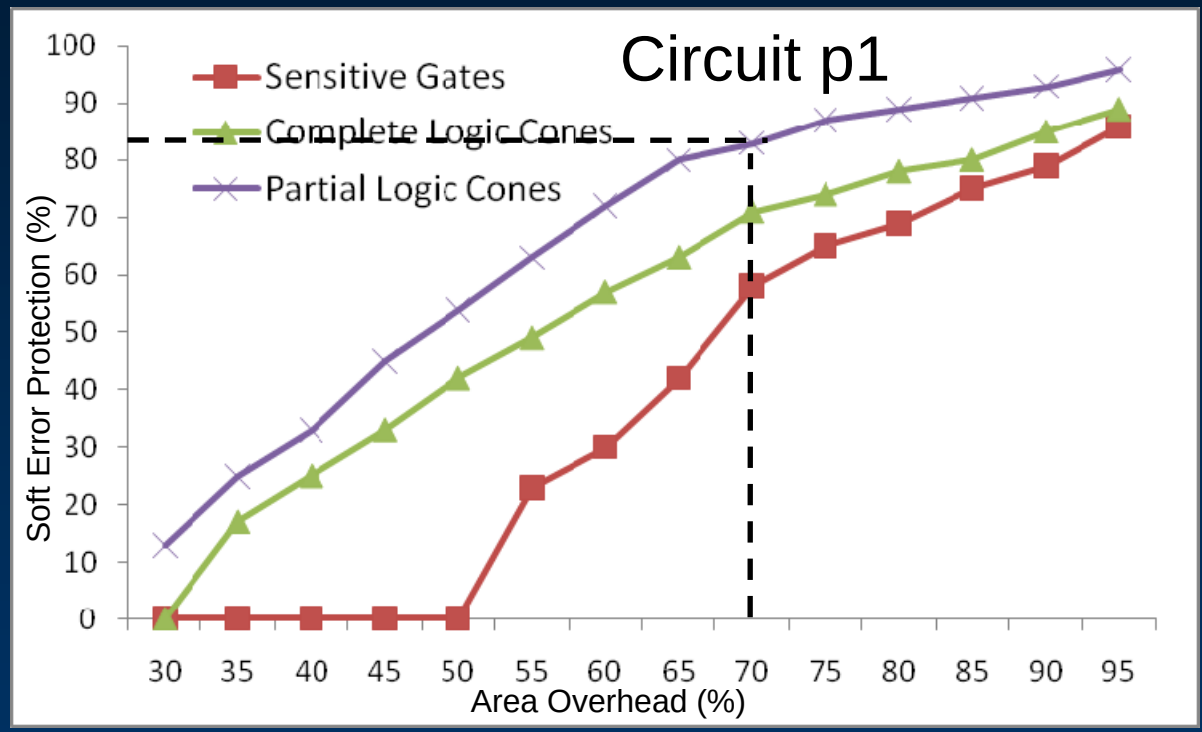
- Achieved tolerance is commensurate with the area overhead
- The partial logic cones mitigation method is consistently better

Experimental Results

Multi-level ABMMs (new release by Columbia Univ.)

Cost:
70%

Tolerance
:
84%



Multi-level implementation significantly improves the tradeoff between area overhead & achieved soft error tolerance

Summary

- Soft error tolerance in ABMMs
  - ➔ Duplication-based solution that improves upon TMR
  - ➔ Cross-coupled C-element structure for state-line protection
- Soft error mitigation in ABMMs
  - ➔ Enables exploration of the trade-off between the achieved soft error tolerance and the incurred area overhead
  - ➔ Driven by soft error susceptibility estimation via hazard-aware asynchronous fault simulator (SPIN-SIM)
  - ➔ Yields 3 progressively more powerful partial duplication options