The family of 4-phase latch controllers

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A systematic way of studying the design-space for untimed, bundled, 4-phase latch controllers.

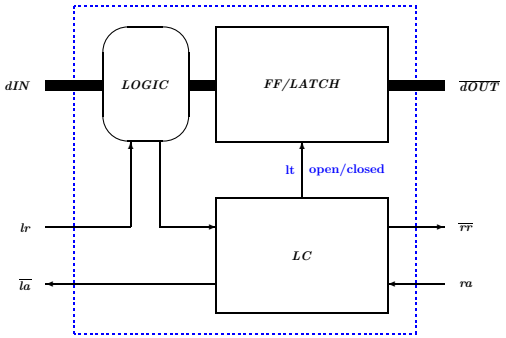
1. *Shape* of the most concurrent protocol.

2. Its family of less-state rich shapes.

3. Categorising/relating the family.

4. Tabulation of pipeline behaviours.

Setting: notation in, $\overline{out}$

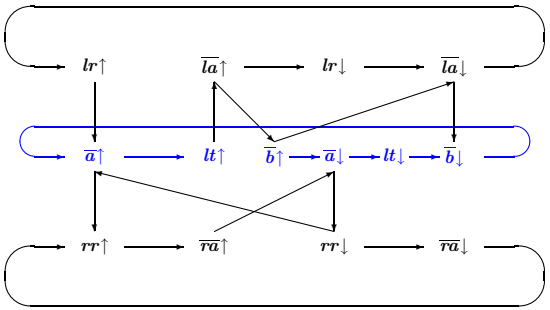


Suitable abstraction for LC behaviours?

We argue that:

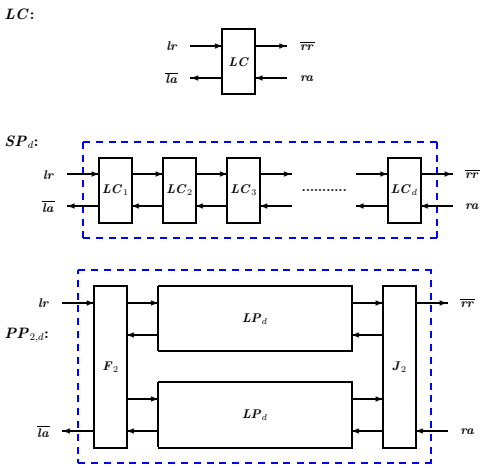
- internal states: implicit part of a spec
- logic: just delays lr (or $\overline{la}$)
- enable: another lateral delay

STG: Furber and Day, sect 6



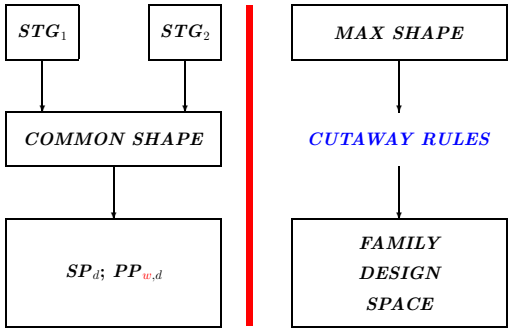
- In our abstractions, internal states a and b are hidden; likewise lt.
- The constraints they impose will remain.
- Each abstraction will have several circuit implementations, each of which have the same pipeline characteristics.

Pipeline models



Outputs $\overline{rr}/\overline{la}$ and Inputs lr/ra

STGs/Abstract Shape/Family



1. Several STG's → same abstract shape.

2. We can compare shapes.

3. We can define the maximal shape
   ... and its derivative family.

Max latch controller protocol

$$L = lr\uparrow \;.\; \overline{la}\uparrow \;.\; lr\downarrow \;.\; \overline{la}\downarrow \;.\; L$$

$$R = \overline{rr}\uparrow \;.\; ra\uparrow \;.\; \overline{rr}\downarrow \;.\; \overline{ra}\downarrow \;.\; R$$

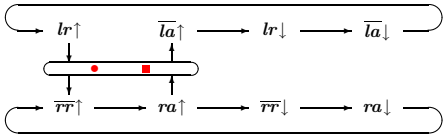
$$LC = (\; L \mid R \;)$$

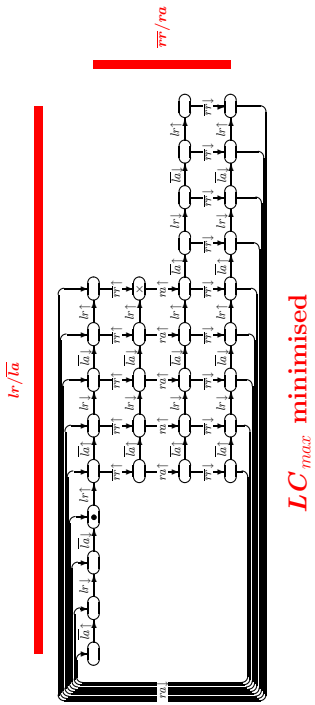
In CCS $lr\uparrow.\overline{la}\uparrow$ is read as
$lr\uparrow$ then some time later $\overline{la}\uparrow$
All possible interleavings are traced

$$L = lr\uparrow \;.\; \blacksquare \;.\; \bullet \;.\; \overline{la}\uparrow \;.\; lr\downarrow \;.\; \overline{la}\downarrow \;.\; L$$

$$R = \bullet \;.\; \overline{rr}\uparrow \;.\; ra\uparrow \;.\; \blacksquare \;.\; \overline{rr}\downarrow \;.\; \overline{ra}\downarrow \;.\; R$$

$$LC_{max} = (\; L \mid R \mid \bullet \mid \blacksquare \;) \setminus \{ \bullet, \blacksquare \}$$





UNTIMED Cutaway Rules

Cheap version: LC_{max}, shape 9599.

o o o • o o o o o
o o o o o
o o o o o o o o o
o o o o o o o o o

1. • same state when quiescent

2. no holes in the state graph

3. always accept an input lr/ra

4. may delay an output $\overline{la}/\overline{rr}$

The Cut-Away Notation

1. *L1001* → shape 8598 10

. o o • o o o o o
o o o o o
o o o o o o o o o
. o o o o o o o o

Left cut-aways constrain $\overline{rr}/ra$.

2. *R0040* → shape 9559 25

o o o • o o o o o
o o o o o
o o o o o . . . .
o o o o o o o o o

Right cut-aways constrain $\overline{la}/lr$.

Cut-Away Notation II

L1001 o R0040 → 8558 **250**

```
. o o • o o o o o
        o o o o o
        o o o o o . . . .
        . o o o o o o o o
```

- L1001 o R0040 (Furber/Day, sect. 6)
- ALL L o R → generates the whole family
- The cutaway options make it trivial to order the family into a lattice

  L_1 o $R_1 \supseteq L_2$ o R_2
  IFF
  $L_1 \supseteq L_2$ AND $R_1 \supseteq R_2$

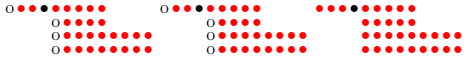
Pipeline categories

Is shape preserved when pipelined?

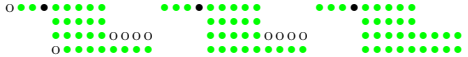
Basic shape | SP_d shape | $PP_{w,d}$ shape

STABLE

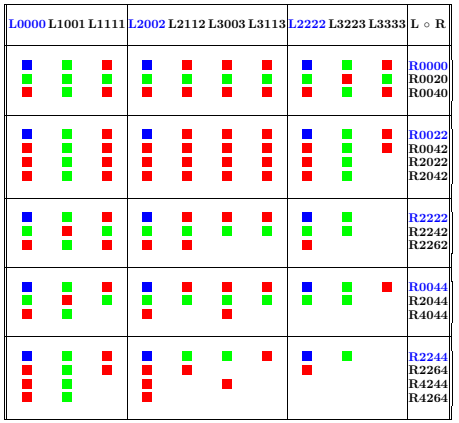
REGULAR



2REGULAR



Protocol categories



- 6 categories emerge:
  - ■: STABLE
  - ■: 2reg
  - : linear

  regular: ■
  O(8): as O(16)
  dead:

Parallel pipelines $PP_{w,d}$

L0000 L1001 L1111	L2002 L2112 L3003 L3113	L2222 L3223 L3333	L ∘ R
■ • • • • • • • •	■ • • • • • • • • • • •	■ • • • • • • • •	R0000 R0020 R0040
■ • • • • • • • • • • •	■ • • • • • • • • • • • • • • •	■ • • • • • • •	R0022 R0042 R2022 R2042
■ • • • • • • • •	■ • • • • • • • • •	■ • • • •	R2222 R2242 R2262
■ • • • • • • •	■ • • • • • • • •	■ • • • •	R0044 R2044 R4044
■ • • • • • • • • • •	■ • • • • • • • •	■ • •	R2244 R2264 R4244 R4264

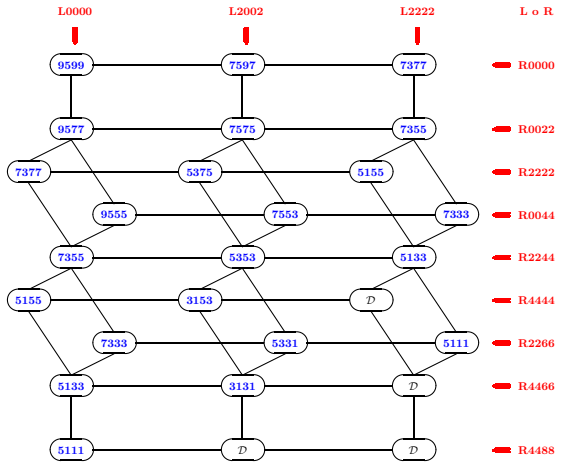
Independent of w.
Same result throughout each block.
Maths says TL; Engineering BR?

Single pipelines SP_2

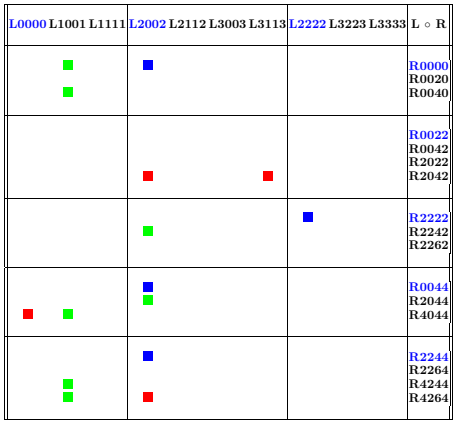
L0000 L1001 L1111	L2002 L2112 L3003 L3113	L2222 L3223 L3333	L ∘ R
48 48 44 48 48 44 44 44 40	44 42 42 40 44 42 42 40 40 38 38 36	40 36 36 40 36 36 36 32 32	R0000 R0020 R0040
44 44 40 42 42 38 42 42 38 40 40 36	40 38 38 36 38 36 36 34 38 36 36 34 36 34 34 32	36 32 32 34 30 30 34 30 $\mathcal{D}$ 32 28 $\mathcal{D}$	R0022 R0042 R2022 R2042
40 40 36 36 36 32 36 36 32	36 34 34 32 32 30 30 28 32 30 $\mathcal{D}$ $\mathcal{D}$	32 28 $\mathcal{D}$ 28 24 $\mathcal{D}$ 28 $\mathcal{D}$ $\mathcal{D}$	R2222 R2242 R2262
40 40 36 36 36 32 36 36 $\mathcal{D}$	36 34 34 32 32 30 30 28 32 $\mathcal{D}$ 30 $\mathcal{D}$	32 28 28 28 24 $\mathcal{D}$ $\mathcal{D}$ $\mathcal{D}$ $\mathcal{D}$	R0044 R2044 R4044
28 28 24 26 26 22 26 26 $\mathcal{D}$ 24 24 $\mathcal{D}$	24 22 22 20 22 20 $\mathcal{D}$ $\mathcal{D}$ 22 $\mathcal{D}$ 20 $\mathcal{D}$ 20 $\mathcal{D}$ $\mathcal{D}$ $\mathcal{D}$	20 16 $\mathcal{D}$ 18 $\mathcal{D}$ $\mathcal{D}$ $\mathcal{D}$ $\mathcal{D}$ $\mathcal{D}$ $\mathcal{D}$ $\mathcal{D}$ $\mathcal{D}$	R2244 R2264 R4244 R4264

■ shapes behave as ■ shapes for d $\geq$ 2.
Many distinct shapes.
Equivalences stay in the same box.

Lattice of stable shapes



Published circuit shapes



Includes: Early; Broadish; Broad

Un-/Semi-/Fully-Decoupled

Normally open/normally closed

What's been done

1. Idea of an abstract design shape and how it composes.
   Each shape may have many implementations but each will maintain the piped behaviour of its shape

2. Family of untimed, bundled protocols derived by cutaways from the most state rich shape.
   Cutaways enable us to order the family.

3. We have classified pipeline behaviours for the whole family of shapes.
   And can predict mixed parallel pipeline behaviour from their cutaways.

What's to be done

1. Circuit chrestomathy and shape cook book.
   Any other circuits out there?

2. Including *lt* signals (goes exponential).

3. Mixed parallel pipelines $\surd$.
   Single pipelines en route.

4. Maths/Engineering interplay and insights.

5. Timed disciplines.

6. $\mathbf{Y}$ (Ken is generating circuits).